MAINTENANCE MANUAL

Model 869

Multi-Channel Pulse Generator Mainframe

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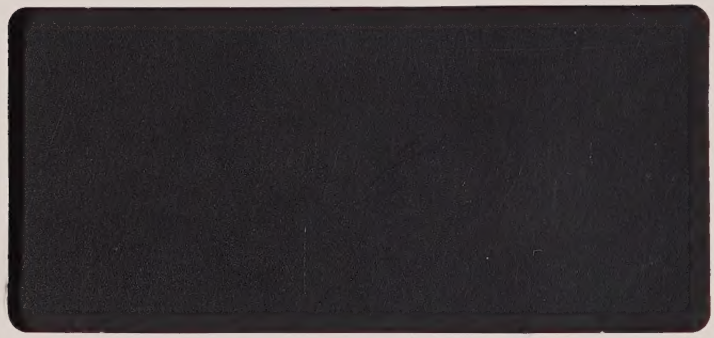

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Multi-Channel Pulse Generator Mainframe

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Instrument Part Number:
1 Channel: 1000-00-0641
2 Channel: 1000-00-0642
3 Channel: 1000-00-0643
4 Channel: 1000-00-0644

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- Don't plug in the power cord until directed to by the installation instructions.
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- Pay attention to the CAUTION statements. They point out situations that can cause equipment damage.

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CONTENTS

SECTION 1 GENERAL DESCRIPTION

1.1 INTRODUCTION 1-1
1.1.1 Plug-In Module Hardware 1-1
1.1.2 System Mainframe Hardware 1-1
1.2 EQUIPMENT DESCRIPTION 1-2
1.2.1 System Architecture 1-2
1.3 MODEL 869 MAINFRAME SPECIFICATIONS 1-4
1.3.1 Outputs 1-4
1.3.2 Inputs 1-4
1.3.3 System Trigger 1-4
1.3.4 Internal 10 MHz Reference 1-4
1.3.5 General 1-5
1.3.6 Modules 1-5
1.3.7 Options 1-5

SECTION2 OPERATION

2.1 INTRODUCTION 2-1
2.2 DETAILED BLOCK/INTERCONNECT 2-1
2.3 FRONT PANEL BOARD 2-2
2.3.1 Function 2-2
2.3.2 Block Diagram Description 2-2
2.3.3 Circuit Description 2-2
2.4 I/O PROCESSOR BOARD 2-6
2.4.1 Function 2-6
2.4.2 Block Diagram Description 2-6
2.4.3 Circuit Description 2-7
2.5 THE REFERENCE/CALIBRATOR BOARD 2-10
2.5.1 Function 2-10
2.5.2 Block Diagram Description 2-10
2.5.3 Circuit Description 2-12
2.6 VME MICROPROCESSOR BOARD 2-19
2.6.1 Function 2-19
2.6.2 Interface With the Main Interconnect Buses 2-20
2.6.3 Block Diagram Description 2-21
2.6.4 Circuit Description 2-25
2.7 THE MAIN INTERCONNECT BOARD 2-34
2.7.1 Function 2-34
2.7.2 Block Diagram Description 2-34
2.7.3 Circuit Diagram Description 2-37

SECTION 3 CALIBRATION

3.1 INTRODUCTION 3-1
3.2 AUTOCAL AND QUICKCAL 3-1
3.3 CALIBRATION REFERENCE SOURCES 3-1
3.4 +2 VREF VOLTAGE ADJUSTMENT 3-2
3.5 10 MHz REFERENCE ADJUSTMENT ADJUSTMENT 3-2

CONTENTS (Continued)

SECTION 4 TROUBLESHOOTING

4.1 INTRODUCTION 4-1
4.1.1 Test Equipment Requirements 4-1
4.2 OPERATIONAL CHECK 4-1
4.2.1 Isolation with 869 Selftest Facitity 4-2
4.2.2 Isolation with 869 AutoCal Facitity 4-3
4.3 POWER SUPPLY TESTS 4-5
4.4 FAULT ISOLATION - NO POWER-UP DISPLAY 4-5
4.5 DISPLAY AND IO BOARD TEST 4-6
4.5.1 Troubleshooting a Fatal Failure 4-6
4.5.2 Display Tests 4-8
4.5.3 Keyboard Tests 4-8
4.5.4 Control Knob Tests 4-8
4.5.5 External I/O (GPIB) Test 4-9
4.5.6 Beeper Test 4-9
4.5.7 Display Viewing Angle Tests 4-9
4.5.8 Backlight Test 4-9
4.6 REF/CAL BOARD TESTS 4-9
4.6.1 Troubleshooting a Fatal Failure 4-9
4.6.2 Internal Oscillator Tests 4-11
4.6.3 Voltage Reference Tests 4-11
4.6.4 Internal Trigger Circuit Tests 4-12
4.6.5 System Trigger Circuit Tests 4-12
4.6.6 Temperature Sensor Test 4-12
4.6.7 Amplitude/Offset Control Circuit Tests 4-12
4.7 VME PROCESSOR BOARD TEST 4-13
4.7.1 Pre-Powerup Check Out 4-13
4.7.2 Test Configuration 4-13
4.7.3 Power-On Test 4-13
4.7.4 Power Suppy 4-13
4.7.5 68000 CPU Bus Test 4-13
4.7.6 CLOCK Circuit Test 4-13
4.7.7 RESET Circuit Tests 4-14
4.7.8 BUS ERROR Circuit Tests 4-14
4.7.9 ROM Tests 4-14
4.7.10 DRAM Tests 4-14
4.7.11 Front Panel Communication Tests 4-15
4.7.12 Real Time Clock Tests 4-15
4.7.13 System Sync Tests 4-15
4.7.14 DFI Circuit Tests 4-15
4.8 UTILITY/GPIB DIAGNOSTIC ROUTINES 4-15

SECTION 5 PARTS AND SCHEMATICS

5.1 DRAWINGS 5-1
5.2 ERRATA 5-1
5.3 ORDERING PARTS 5-1

ILLUSTRATIONS

Figure		Page
1-1	Model 869 Mainframe with Four 680-03 Plug-in Modules	1-1
1-2	Model 869 System Interconnection	1-2
1-3	Model 869 System Architecture	1-3
2-1	Model 869 Block/Interconnect Diagram	2-1
2-2	Front Panel Board Block Diagram	2-2
2-3	Keyboard Matrix	2-4
2-4	Dial Cursor Control Encoding	2-5
2-5	Viewing Angle	2-5
2-6	I/O Processor Board Block Diagram	2-7
2-7	Microprocessor Timing Diagram	2-8
2-8	Reference Calibrator Board Block Diagram	2-11
2-9	Trigger Control Gateable Oscillator	2-16
2-10	Internal Trigger Circuit	2-16
2-11	DVM and Gain Select Block Diagram	2-17
2-12	Counter Logic Diagram	2-18
2-13	Sample and Hold Circuit	2-19
2-14	VME Microprocessor Board Bus Interface	2-20
2-15	VME Microprocessor Board Block Diagram	2-22
2-16	System Clock Timing	2-25
2-17	System Reset Timing	2-26
2-18	PAL Interconnection Diagram	2-27
2-19	Interrupt Response Timing	2-29
2-20	VME Bus Arbitration Timing	2-30
2-21	DTACK Timing	2-31
2-22	Motherboard Block Diagram	2-35
2-23	Typical VME Bus Signal Line	2-35
2-24	System Timing Bus	2-36
2-25	Calibration Bus Voltage Measurement Interconnections	2-36
2-26	Calibration Bus Frequency Measurement Interconnections	2-37
2-27	DAC Bus	2-37
4-1	Power Supplies and Board Locator	4-4

TABLES

Table		Page
2-1	Display Module Pin Description	2-3
2-2	I/O Processor Board Memory Map	2-9
2-3	Dual Port RAM Allocation	2-13
2-4	16k Zone Address Decoder	2-14
2-5	4k Zone Address Decoder	2-14
2-6	Decoders U4 and U9	2-14
2-7	Control Latch Enables	2-15
2-8	VME Signal Exceptions	2-21
4-1	Initial Fault Isolation	4-1
4-2	Required Equipment/Fixtures	4-1
4-3	Troubleshooting Error Codes	4-4
4-4	Power Supply Voltage Distribution	4-4

SECTION 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The Wavetek model 869 (hereafter defined as the model 869) multi-channel pulse generator, shown in figure 1-1, is a modular, bench or rack mounted test instrument. This manual provides maintenance information on the mainframe system only. Operational information for the 869 Multi-Channel Pulse Generator, and maintenance information for the model 680-03 High Performance Pulse Generator module is given in separate manuals.

The model 869's hardware consists of:

1. Plug-in pulse generator modules (model 680-03).
2. Permanent system mainframe hardware which controls and supports the modules.

1.1.1 Plug-in Module Hardware

One to four model 680-03 pulse generator channel modules are loaded into the mainframe, using two module slots per channel. All unused module slots must contain a blank module for bus continuity, radiation control and air path control. Refer to the 869 Operator's Manual and the 680-03 Maintenance Manual for detailed information on the pulse generator modules.

1.1.2 System Mainframe Hardware

The mainframe system provides support resources consisting of a switching power supply module, a front panel and a microprocessor, reference/calibrator, input/output (I/O) processor and motherboard. This set of mainframe resources and circuit blocks is the subject of the remainder of this manual.

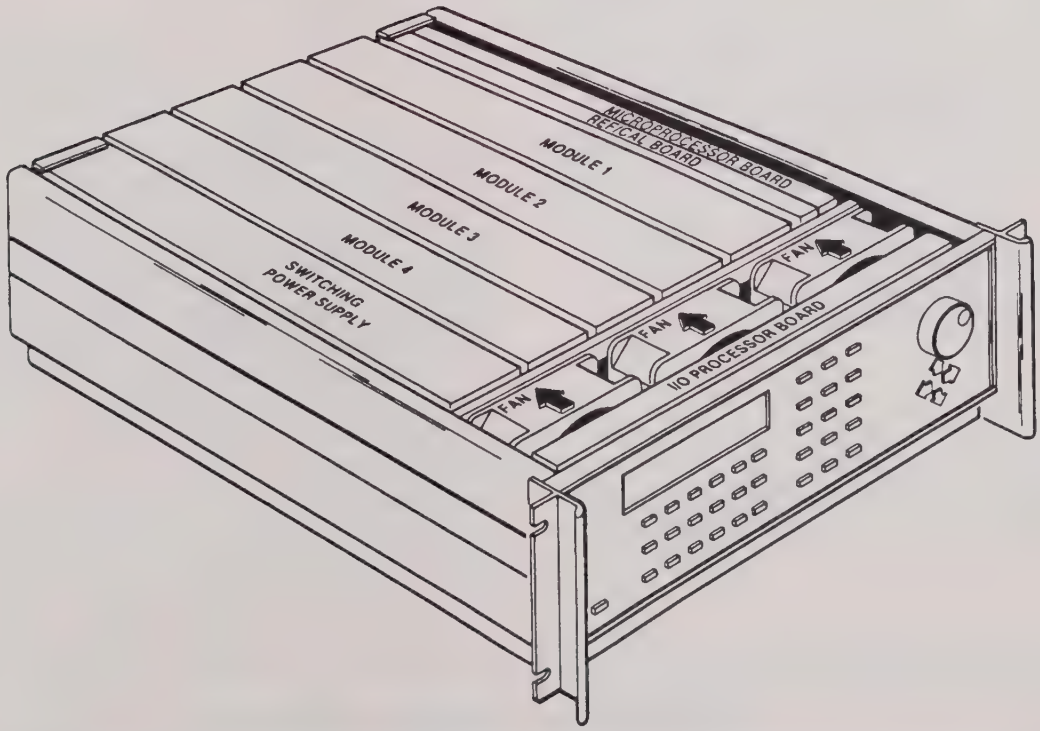


Figure 1-1. Model 869 Mainframe with Four 680-03 Pulse Generator Modules

1.2 EQUIPMENT DESCRIPTION

Figure 1-2 illustrates the interconnection of the 869 . The instrumentation controller initializes and loads the 869 with test setups which automatically evaluate equipment under test.

1.2.1 System Architecture

Figure 1-3 illustrates the 869 block diagram. As previously described, the permanent system mainframe hardware supports and interfaces with the pulse generator modules used or needed for a wide range of signal and timing applications.

The **I/O Processor Board**, containing a 6803 microprocessor, enables the user to communicate with the 869 either from the keyboard (manual operation) or from the External I/O bus (remote operation). The programming commands from either source are routed to the **VME Microprocessor Board** which contains a 68000 microprocessor, that analyzes these commands to call-up menus or execute command setups. The I/O processor board uses a liquid crystal display (LCD) to give a visual indication of front panel operation and permits the user to view menus, which define labels for function keys, current instrument parameters and warning responses of keyboard error or erroneous operation.

The **Reference/Calibrator** (Ref/Cal) **board** provides certain reference resource signals and voltages which are used by the permanent mainframe system hardware to calibrate the installed pulse generator modules. In addition, the Ref/Cal board is controlled by a 6803 microprocessor which interfaces with the microprocessor board through a local bus. The specific resources

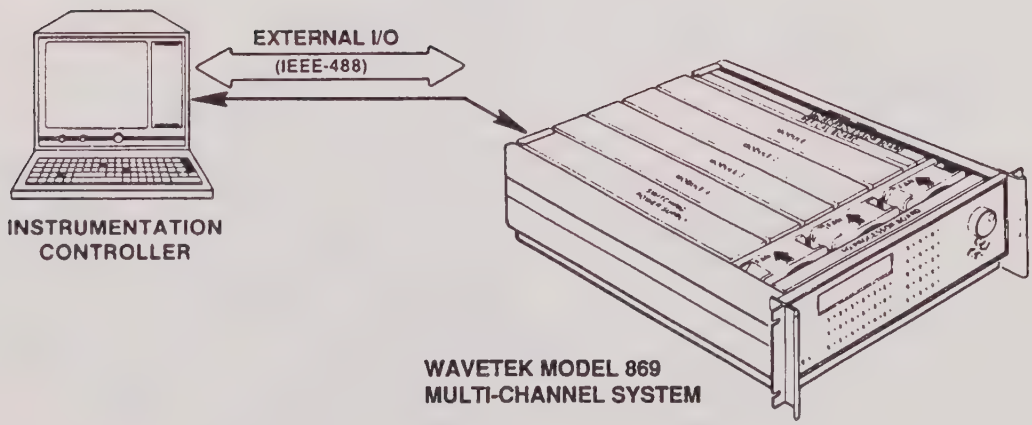


Figure 1-2. Model 869 System Interconnection

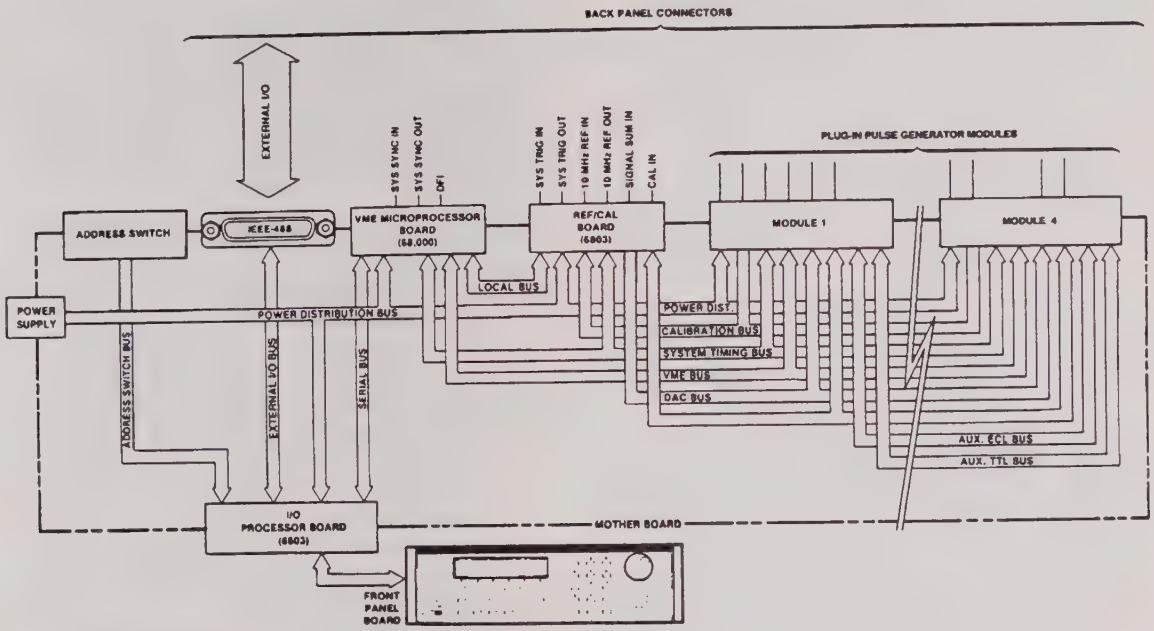


Figure 1-3. Model 869 System Architecture

provided by the Ref/Cal board are:

1. A DVM (3-1/2 Digit) used for calibration and diagnostics of the modules.
2. A frequency counter (100 MHz) which is also used for calibration and diagnostics of the modules.
3. A system trigger source which can be, through choice, either internally generated or externally supplied. The external trigger is definable as far as slope (either positive or negative edge causes trigger), level (what amplitude causes the trigger), event (a selectable number of events causes trigger) and delay (after a certain amount of time causes a trigger).
4. A 10 MHz oscillator reference frequency which can be selected as being either internally generated or externally supplied. This signal provides a clock frequency for logic circuits and also appears at the back panel as a 10 MHz, 50Ω TTL output.
5. A highly accurate and stable +10V and -10V reference voltage for the permanent mainframe and plug-in modules.
6. A 16-bit output sampled digital to analog converter (DAC) that provides high resolution control voltages to the modules for the control of module parameters.

The eight layer **Main Interconnect Board** not only provides all the necessary interfacing between the mainframe system resources and plug-in modules, but also supports communication paths between the modules themselves. A listing of these internal interfacing busses and their function is given below:

1. External I/O Bus — This bus is connected between the IEEE-488 connector on the rear panel and the I/O processor board and provides the communication path between the 869 and the external instrumentation controller.

   NOTE

   Except for the system address, the mainframe is transparent to the External I/O bus commands. The modules within the mainframe (module 1 through 8) receive commands and data from the bus and respond to the external device over the bus.

2. VME Bus — Used by the microprocessor board to input and output command data to the option modules, this bus is basically an extension of the 68000 microprocessor.
3. Local Bus — This bus provides a communication link

between the microprocessor board and the Ref/Cal board.

4. System Timing Bus — This bus entails three timing signals:
   a. A 10 MHz clock for use by logic circuitry throughout the 869.
   b. A system synchronization (SSYNC) line which can provide the necessary timing signals to ensure all modules or instruments are in sync with one another.
   c. A system trigger (STRIG) line which initiates certain events to occur when the trigger mode is selected. This signal can be either internally generated or externally supplied.
5. Calibration Bus — This Ref/Cal input only bus is used to supply a sampling of voltages and frequencies from each of the plug-in modules for automatic calibration and built-in test (BIT) or self diagnostics.
6. DAC Bus — This Ref/Cal output bus consists of 16 high resolution analog control lines which drive the modules to control the instrument's variable programmed parameters.
7. Analog Signal Bus — This 7 line bus providing the distribution of analog signals, is not utilized in the model 869.

The power supply provides supply voltages for the entire 680 via the power distribution bus. Voltages provided are: +5V, -5V, +15V, -15V, +24V, -24V, +5V isolated and a +24V unregulated supply.

1.3 MODEL 869 MAINFRAME SPECIFICATIONS

1.3.1 Outputs

System Sync Output and System Trigger Output: Source selected by Master/Slave/Independent keys.
Signal Level: 0.2 to 1.0V into 50Ω typ.
Transition Time: <10 ns.
Output Impedance: 50Ω.

10 MHz Reference Output: 0.2 to 2.4V into 50Ω (TTL for >10 kΩ).
Transition Time: <10 ns into 50Ω.
Output Impedance: 50Ω.

DFI Output: (Discrete Fault Indicator.) Relay contact closure to indicate fault condition for power off, microprocessor failure or over-temperature.

1.3.2 Inputs

System Sync Input: Selected by Slave mode TTL levels required.
Input Impedance: >1 kΩ.
Bandwidth: >20 MHz.

System Trigger Input: A signal between 1 Vpp and 10 Vpp will trigger the system.
Frequency: <20 MHz for Normal trigger and <5 MHz for Delayed and Event trigger.
Transition Time: <50 ms.
Minimum Pulse Width Requirement: 25 ns.
Impedance: >1 kΩ.

10 MHz Reference Input: 1 Vpp min to 10 Vpp.
Range: >±5% centered on 10 MHz .
Input Impedance: >1 kΩ.

Calibration Input: Used to calibrate the internal DVM. ±4 Vdc ±0.1 mV.

1.2.3 System Trigger

External Trigger
Modes: Normal, Time Delay, Event Delay.
Delay Range: 100 ns to 10s.
Resolution: 100 ns.
Accuracy: ±(1% + 30 ns).
Event Delay: 2 to 1 x 10^7 events, selectable slope.

Internal Trigger
Frequency Range: 0.01 Hz to 10 MHz.
Resolution: 4 digits.
Accuracy: ±0.05%.

1.3.4 Internal 10 MHz Reference

Accuracy: ±1 ppm, 15° to 35°C.
Stability: ±1 ppm/year (typ).

1.3.5 General

Stored Settings: 99 stored settings are provided by the chassis. These are allocated as needed between the chassis and installed modules.

GPIB Programming: The software interface uses a subset of the IEEE-488.2 Draft Standard, "Codes, Formats, Protocols and Common Commands for use with ANSI/IEEE Std 488.1-1987, " IEEE Standard Digital Interface for Programmable Instrumentation," version dated 27 March 1987 as a general guide.
IEEE-488 Subsets: SH1, AH1, TE6, LE4, SR1, RL1, PP0, DC1, DT1 and E1.

Environment
Operating Range: 0° to +50°C.
Relative Humidity: 95% non-condensing at 25°C.
Altitude: 10,000 ft.
Storage: –40° to +75°C, 40,000 ft.

Dimensions:
Height; 17.78 cm (7 in.)
Length; 54.6 cm (21.5in.)
Width; 44.5 cm (17.5 in.)
Supplied with rack mount adapters.

Weight:
Chassis only; 17.3 kg (38 lb) net
With 1 module; 22.9 kg (51 lb) net
With 2 module; 24.9 kg (55 lb) net
With 3 module; 26.9 kg (59 lb) net
With 4 module; 28.9 kg (64 lb) net
Add 3.6 kg (8 lb) for shipping weight.

Power: 90 to 126.5 Vac, 200 to 250 Vac, 48 to 66 Hz.
<50 watts chassis only,
Add 50 watts for each module installed.

Extender Cards: Four 96 pin cards are required per module.

1.3.6 Modules

Model 680-00: Blank Module
Two blank modules are supplied for each unused pulse generator channel. They provide continuity for the interrupt daisy chain and for proper cooling.

Model 680-03: 100 MHz Module
A 100 MHz, 10 Vpp Pulse Generator module, with variable transition time control. Up to four channels, operated independently or slaved, can be installed in the same chassis.

1.3.7 Options

Model 680-010: MATE-CIIL Interface
Contact factory for availability.

SECTION 2
OPERATION

2.1 INTRODUCTION

This section of the manual is primarily intended as a technical service aid for the individual with some background in electronics, especially microprocessor based systems. The following block diagrams and circuit descriptions along with the schematic diagrams in Section 5, should aid you in both understanding and servicing the model 869.

2.2 DETAILED BLOCK/INTERCONNECT

Figure 2-1 illustrates the block/interconnect diagram of the model 869 mainframe chassis. The following sections will discuss each block in greater detail; however, this diagram should help you gain a clear understanding of the complete model 869 system interconnection.

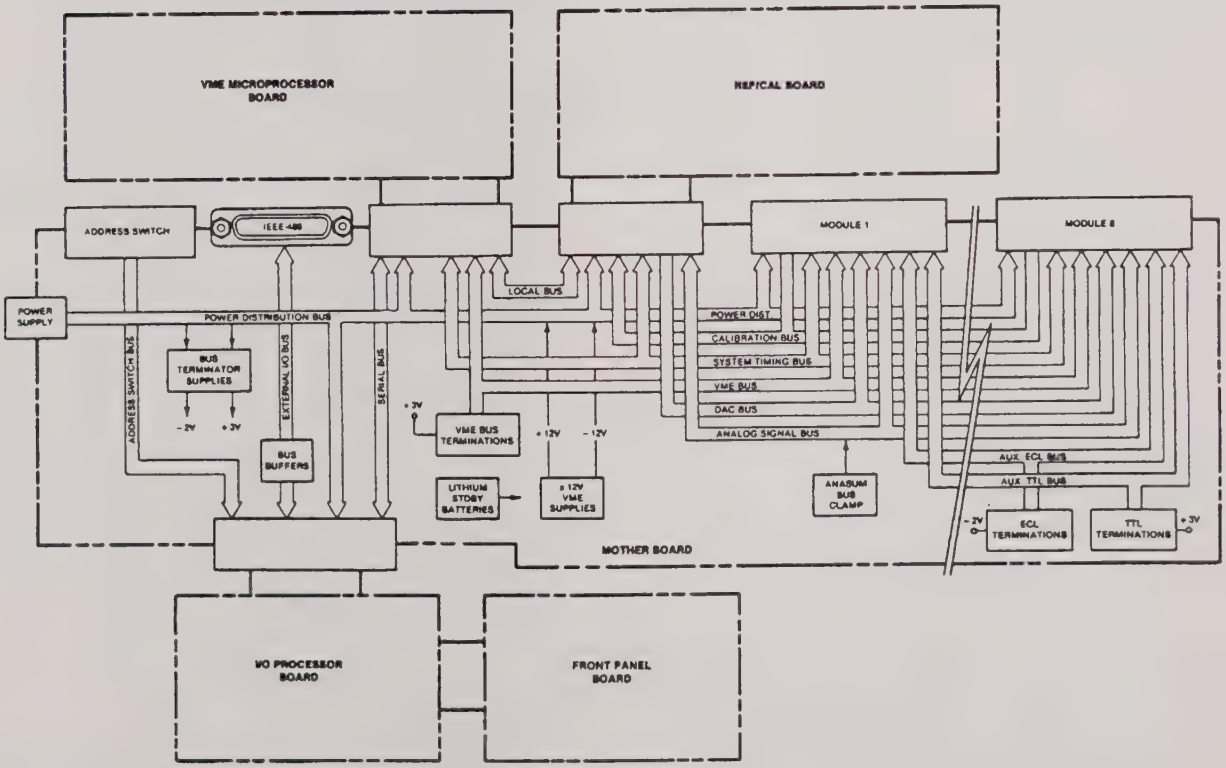


Figure 2-1. Model 869 Block/Interconnect Diagram

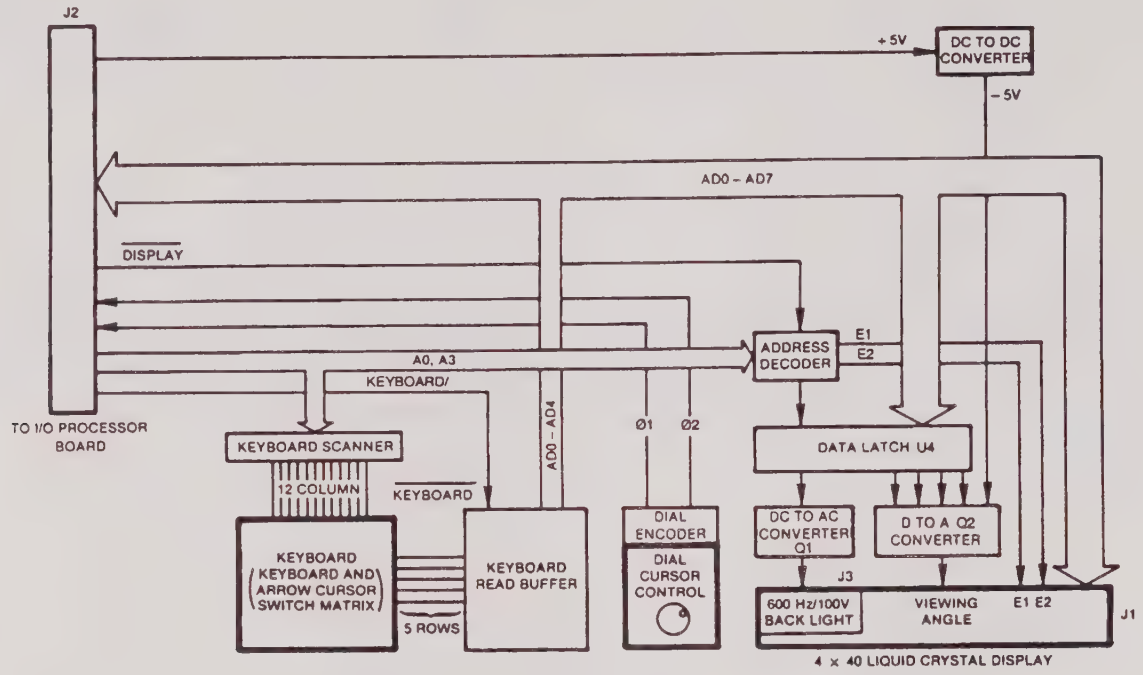


Figure 2-2. Front Panel Board Block Diagram

2.3 FRONT PANEL BOARD

2.3.1 Function

The display and keyboard are the local means of communication between the user and the model 869 system. Specifically, the keyboard allows the user to step through menu trees, choose operating modes, enter parameter values and control the cursor position. The display provides the user with both status and control information such as different menus, operating modes, parameters, error messages and cursor position. The two cursor controls (arrow and dial) can be used, dependent on user preference, to vary any numerical values.

2.3.2 Block Diagram Description

Figure 2-2 illustrates the block diagram of the model 869's front panel board. Power and data communication is via connector J2 which is plugged into the I/O Processor Board. The 6 soft, 6 global, 6 module, 15 decimal and 4 arrow cursor keys (37 in total) are scanned and encoded by a keyboard scanner and read buffer which is enabled by the KEYBOARD/ line from J2. The key closure information is passed back via the address-data lines (AD0-AD4) to the 6803 microprocessor on the I/O Processor Board where it will determine which key has been activated. The dial cursor is directly coupled into a dial encoder which produces a two phase signal that is also decoded in the I/O Processor Board to determine the dial direction and amount of rotation. The 40-character, 4-line liquid crystal display (LCD) is a complete display system with a built in microprocessor, ROM, RAM, back light and driver. An address decoder, which is enabled by the DISPLAY/ line from the I/O Processor Board, is used to clock the display data latch. The address decoder also supplies the display package with E1 and E2 control lines that govern whether the top (E1) or bottom (E2) two display lines of the four line display are enabled. The data latch drives both a dc-to-ac inverter that excites an electroluminescent lamp within the display module for back lighting, and a digital-to-analog converter (DAC) that through software control can be made to vary the display viewing angle.

2.3.3 Circuit Description (Drawing Number 0103-00-3124)

All communication into and out of the board is through the connector J2 (schematic location B8-D8) which plugs into the I/O processor board discussed in section 2.4. Power to the front panel board appears on J2 pins 3, 4, 5, 6 and 7 furnishing +5V to all circuits (VCC and VDD) on the board.

The keyboard (schematic location B4-B7) is arranged in a 12-column by 5-row matrix, as simplified in figure 2-3. With no key depressed, the row lines which connect to the keyboard read buffer U6 pins 2, 4, 6, 8 and 11 are pulled high by the 10 kΩ pull-up resistors in the resistor pack RN1.

During the key scanning routine, the 6803 I/O microprocessor sends out a set of consecutive addresses (A0-A3) that drive the keyboard scanners U7 and U8. This pulses low each of the 12 column lines in sequence, as seen in figure 2-3. Every time a low level is sequenced, the row lines 1 through 5 are read onto the address-data bus lines AD0-AD4 out of the board on J2 and into the 6803 I/O microprocessor. Figure 2-3 illustrates an example of one of the switches in the switch matrix, in this case the number 2 switch which is at the intersection of column 8 and row 3. A key closure will pulse low a normally high row line and it is the unique combination of column line address and row line address that enables the I/O microprocessor to determine which key has been pressed. The key scanning takes place so rapidly that several complete scans are made during even the shortest key press.

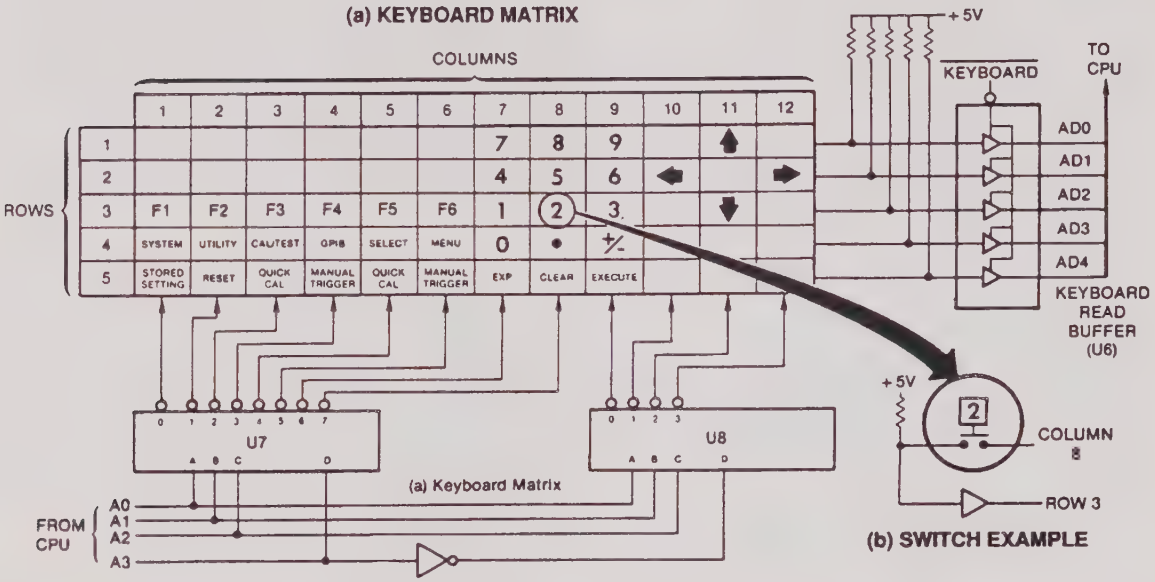
As detailed in figure 2-3, U7 is enabled by a low on A3 and then A0 through A2 are used to sequence columns 1 through 8. A3 then goes high, enabling U8, which is then addressed by A0 through A2 to sequence through the remaining columns 9 to 12.

The dial cursor control, unlike the arrow cursor control and other keys, is encoded separately by DE1 (schematic location C5) which produces a two-phase signal labeled Ø1 and Ø2. The phase relationship between the two is used by the 6803 on the I/O Processor Board to determine the direction in which the knob is being turned. The number of pulses being produced indicates the amount of rotation. Referring to figure 2-4, the dial encoder (DE1) will cause Ø1 to lag Ø2 when the dial is turned clockwise and Ø1 to lead Ø2 when the dial is turned counterclockwise.

The 40-character 4-line liquid crystal display (DSP1) is a complete ASCII compatible display system with a built-in 192-character generator ROM (schematic location 2C). Also included within this package is a CMOS microprocessor and a 160-character (4-line x 40-character) RAM, which is loaded via the data bus (DB0-DB7) with ASCII values whose code determines the character generated, and whose position in RAM governs the characters position on the display. Table 2-1 describes the function of the display module pins.

Table 2-1. Display Module Pin Description

Pin Name	Input/Output	Function
VSS		Ground: 0V
VDD		Power Supply: +5V.
VO	Input	Viewing Angle Adjustment.
RS	Input	Signal to Select Registers
		"0": Selects instruction register (for write) or address counter (for read).
		"1": Selects data register (for read or write).
R/W	Input	Signal to Select either read or write.
		Operation.
		"0": Write operation (CPU LCD module).
		"1": Read operation (LCD module CPU).
E1	Input	Selects upper 2 lines of the 4 line display.
E2	Input	Selects lower 2 lines of the 4 line display.
DB0-DB7	Input/Output	Tri-state bidirectional active high data bus. This bus is used for data exchanges between the CPU and the LCD module.



IC	Columns Scanned
U7	1 through 8
U8	9 through 12

A3	Selects
0	U7
1	U8

COLUMNS

Time	1	2	3	4	5	6	7	8	9	10	11	12
	0	1	1	1	1	1	1	1	1	1	1	1
	1	0	1	1	1	1	1	1	1	1	1	1
	1	1	0	1	1	1	1	1	1	1	1	1
	1	1	1	0	1	1	1	1	1	1	1	1
	1	1	1	1	0	1	1	1	1	1	1	1
	1	1	1	1	1	0	1	1	1	1	1	1
	1	1	1	1	1	1	0	1	1	1	1	1
	1	1	1	1	1	1	1	0	1	1	1	1
	1	1	1	1	1	1	1	1	0	1	1	1
	1	1	1	1	1	1	1	1	1	0	1	1
	1	1	1	1	1	1	1	1	1	1	0	1
	1	1	1	1	1	1	1	1	1	1	1	0

(c) KEYBOARD SCANNING

Figure 2-3. Keyboard Matrix.

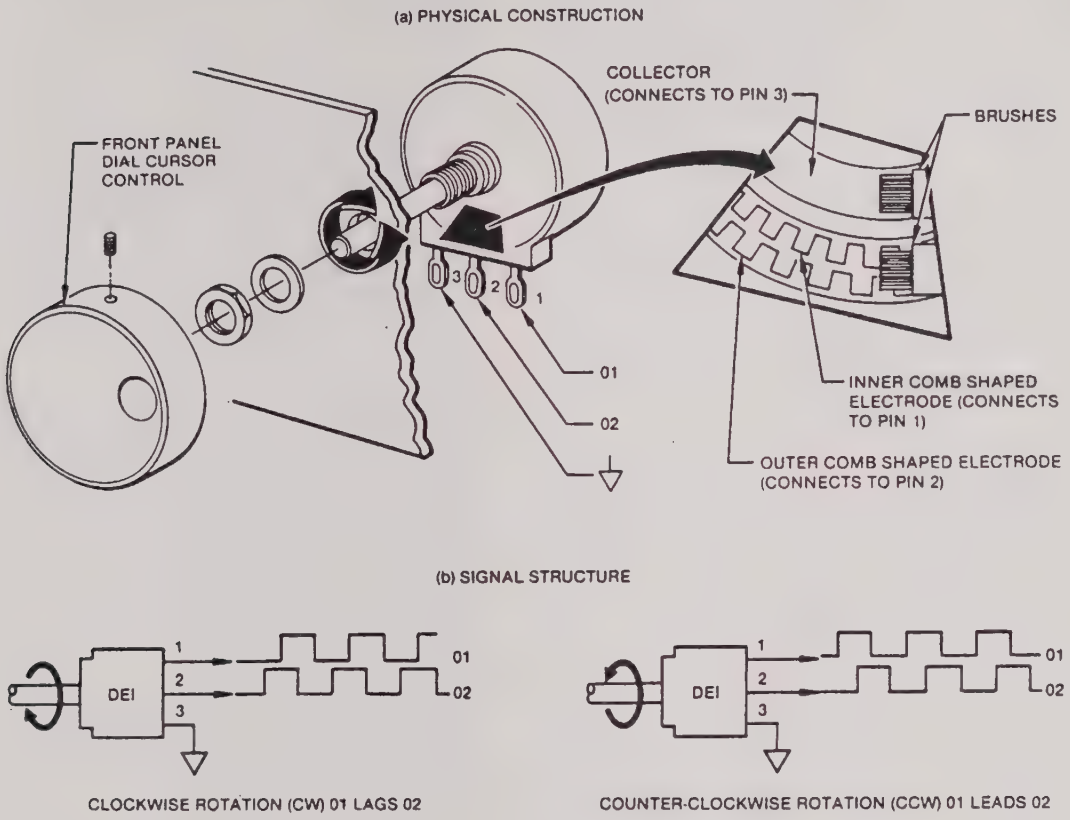


Figure 2-4. Dial Cursor Control Encoding.

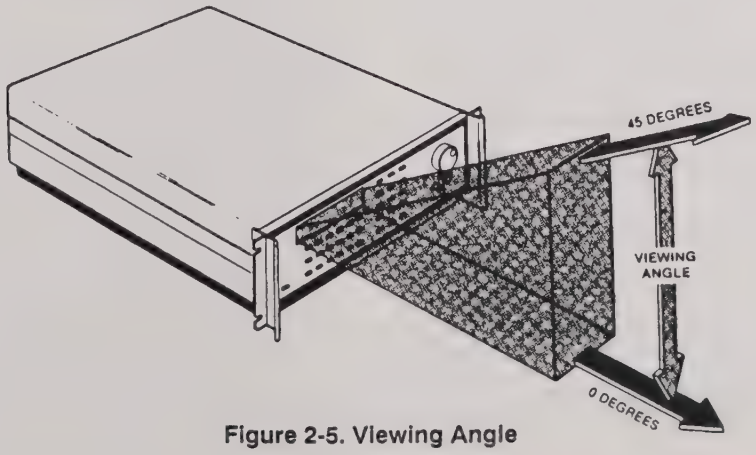


Figure 2-5. Viewing Angle

Referring to the schematic diagram, notice that an address decoder (U1 — schematic location D6) is used to supply one of three enable signals only when the address decoder itself has been enabled by the DISPLAY/ line from the I/O Processor Board. U1 pin 15 (Y0) output drives DSP1 pin 9, and when high will enable the upper two lines of the four line display.

Similarly, U1 pin 14, when selected, will go low and drive DSP1 pin 10 with a high due to the inverter U2B. This input will select the lower two lines of the 4-line display. The third output of the address decoder, U1 pin 13, is used to clock data latch U4 pin 11. The latched data will drive two circuits on the output of U4: a 4-bit digital to analog converter made up of R1, 2, 3, 4, 6, 7 and Q2 (schematic location C3) and a dc-to-ac inverter made-up of Q1, T1 and C6 (schematic location C2).

The 4-bit DAC circuit drives pin 13 (Vo) of the display which, based on the input voltage, will vary the display viewing angle. In order to achieve the viewing angle desired, (0 to 45° as seen in figure 2-5) a voltage swing from 0 to approximately -3V is required. A negative supply voltage for the DAC is supplied by U3 which produces a -5V output at pin 5 and C2 for a +5V input to pin 8. The -5V output is connected to both R7 and Q2 collector (schematic location C3).

The four outputs (Q1 through Q4) of the data latch (U4) set one end of the resistors R1 through R4 to TTL low or high. These resistors, along with R7, provide a voltage divider to the -5V supply. There will be one of16 possible voltage levels (most positive when Q1 through Q4 are all high) at the base of Q2, emitter follower, which is buffered and applied to the Vo input of DSP1 (pin 13). The data latch (U4) is also used to drive transistor Q1, which saturates and passes +5V to the input of the DC-to-AC inverter whenever a logical 0 is applied to its base.

The +5V input is filtered by C6 and converted to approximately 100V/600 Hz ac output that drives pin 1 and 3 of DSP1 to turn on the backlight.

CR1 is the power indicating LED on the front panel and is turned on whenever +5V power is present. R10 functions as a current limiting resistor for CR1.

2.4 I/O PROCESSOR BOARD

2.4.1 Function

The 6803 I/O Processor Board interfaces the local keyboard display and remote External I/O bus with the model 869 system. Specifically, the board will interface the local operator using the keyboard and display or the remote operator using an instrumentation controller via the External I/O bus with the main microprocessor (VME) board.

2.4.2 Block Diagram Description (Figure 2-6)

The 6803 microprocessor operating in its expanded multiplexed mode (mode 2), is the heart of this board and the front panel board. The 6803 communicates with the main microprocessor board through the serial communication port 2 which drives two optical isolators and a serial bus on the motherboard. The optically coupled isolators transmit and receive data, a master reset and a clock, while isolating the External I/O bus ground from the model 869 circuit ground.

An address latch is used to demultiplex the address information from the time multiplexed address data bus. The address decoder analyzes the address bus and selects one of five outputs: an 8K x 8 RAM, an 8K x 8 ROM, a General Purpose Interface Adapter (GPIA), the front panel boards keyboard, or display.

The setting of an 8-bit DIP switch on the rear panel (address) is communicated to the 6803 via the address switch bus and address switch buffer when it is enabled by the GPIA.

The General Purpose Interface Adapter (GPIA) handles all of the data transfer and handshake protocol between External I/O bus and the model 869, or more specifically the 6803 I/O processor.

The External I/O standard is a bit-parallel, byte-serial bus structure designed for communication to and from intelligent instruments. Using this standard many instruments may be interconnected, remotely and automatically controlled or programmed. Data may be taken from, sent to, or transferred between instruments. An instrumentation controller dictates the role of each device by making the attention line true and sending talk or listen addresses on the instrument bus data lines. The devices that have matching addresses, as set-up by the address switch, are activated.

The GPIA operates in conjunction with the standard IEEE-488 bus driver IC's that are located on the motherboard.

This board also contains the dual encoder logic which generates a direction level and knob clock from the Ø1 and Ø2 clocks sent from the front panel board via connector J1.

The logic necessary to generate a beep is also found on this board and activated by the 6803.

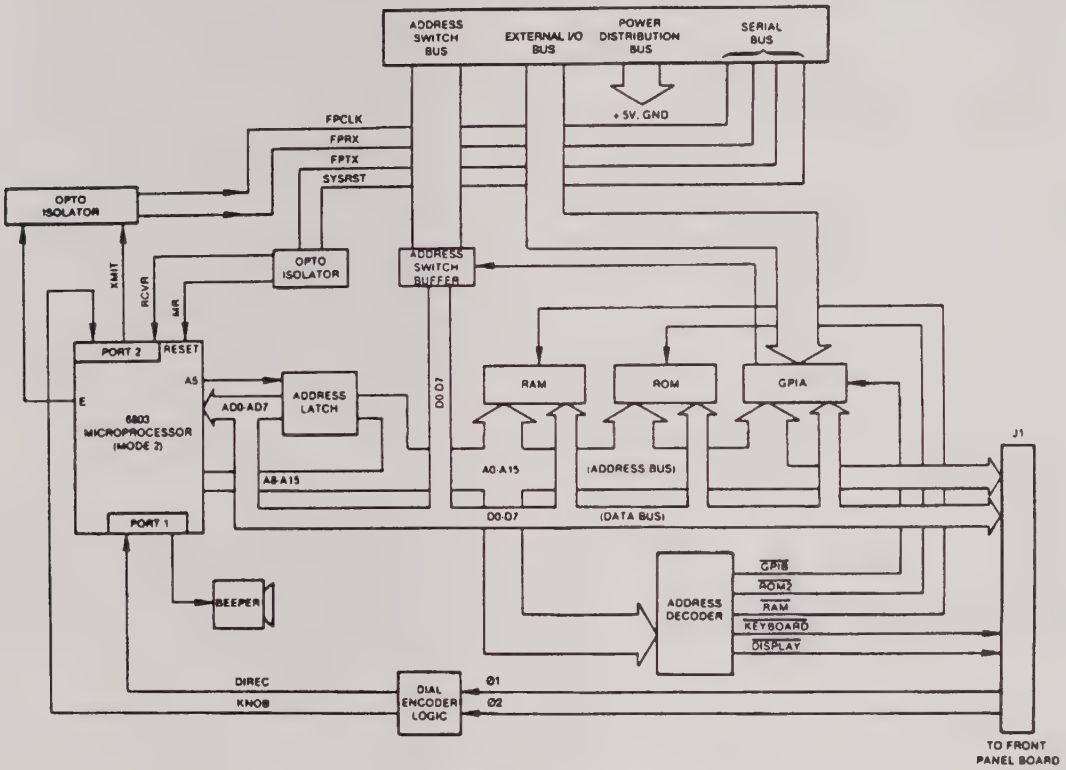


Figure 2-6. I/O Processor Board Block Diagram.

2.4.3 Circuit Description (Drawing Number 1104-00-3236)

2.4.3.1 Microprocessor (Schematic sheet 1, location 7C)

The 6803 microprocessor (U1) is an 8-bit microcomputer that can be hardware programmed into one of eight different operating modes. The operating mode selected controls the configuration of pins 18 through 40. The remaining 22 pins of the 40-pin package are not dependent on the operating mode. The 6803 microprocessor used in the model 869 I/O Processor Board is operated in its expanded multiplexed mode (mode 2). In this mode: port 3 (P30-P37) functions as a time multiplexed address/data bus; port 4 (P40-P47) as the high byte of the address bus and pins 38 and 39 as the read/write (R/W) and address strobe (AS) lines respectively. This operating mode is asserted at RESET by the logic levels on P20, P21 and P22 from a five-bit I/O port. Mode 2 is selected by applying, a low, high, low, respectively on pins 10, 9 and 8 during the positive edge of RESET. This is achieved as P20 is driven by KNOB which is normally high, P21 is permanently pulled high by RN1, and P22 would be pulled low due to the absence of a clock (CLKX1) at the time of a master reset (MR).

A clock oscillator and divider circuit within the microprocessor uses an external 8 MHz crystal connected between XTAL1 and XTAL2 (U1-2,3) to generate a 2 MHz internal phase one clock (Ø1) and external phase two (Ø2) system enable clock that appears at U1-40 (E).

The microprocessor responds to three hardware interrupts: master reset (RESET — pin 6) that initializes the microprocessor, the interrupt request line (IRQ — pin 5) which is used by the external interface to signal the 6803, and a non-maskable interrupt (NMI — pin 4) which is not used.

Serial communication with the main microprocessor on the VME board is achieved through P22, P23 and P24 (pins 10, 11 and 12) of the 6803 via optically coupled isolators.

Figure 2-7 shows the approximate timing for major bus signals. Based on a 2 MHz output clock frequency, the E clock period is 0.5 μs.

In summary, the input 6803 microprocessor performs the following input interfacing functions:

1. Operator Interfacing
   - Operates Menu trees.
   - Checks keyboard-entered parameters/modes against limits.
   - Displays error messages for illegal commands.

2. External I/O Bus Interfacing
   - Strips parameters/modes from command strings.
   - Checks entered parameters/modes against limits.
   - Loads listen and service request (SRQ) buffers.
3. Loads legal parameter/modes into pending commands register.
4. Executes (sends to main microprocessor on VME board) pending commands.
5. Transmits cursor knob/arrow changes to main microprocessor board.

2.4.3.2 Address Latch (Schematic sheet 1, location 5D)

An octal D-type latch (U2) is used to demultiplex the address information from the time multiplexed address/data bus (AD0-AD7). Referring back to the timing diagram in figure 2-7, the address strobe signal goes high when an address appears on the multiplexed address/data bus. This address strobe signal is used to clock the address latch (U2-11) which, since it is level clocked, will pass the lower byte of the address directly through to the output, as the three state output control (U2-1) is permanently enabled. When the address strobe (AS) signal goes inactive (low) the lower byte of the address (A0-A7) will be held at the output of U2. From there it addresses the decoder, ROM, RAM, External I/O bus interface, and front panel board.

2.4.3.3 Address Decoder (Schematic sheet 1, location 7B)

Decoding of the addresses from the microprocessor is achieved by U4, a Programmable Array Logic (PAL) circuit. A4 through A15 are applied to pins 1 through 13; and they are used to select one of five outputs.

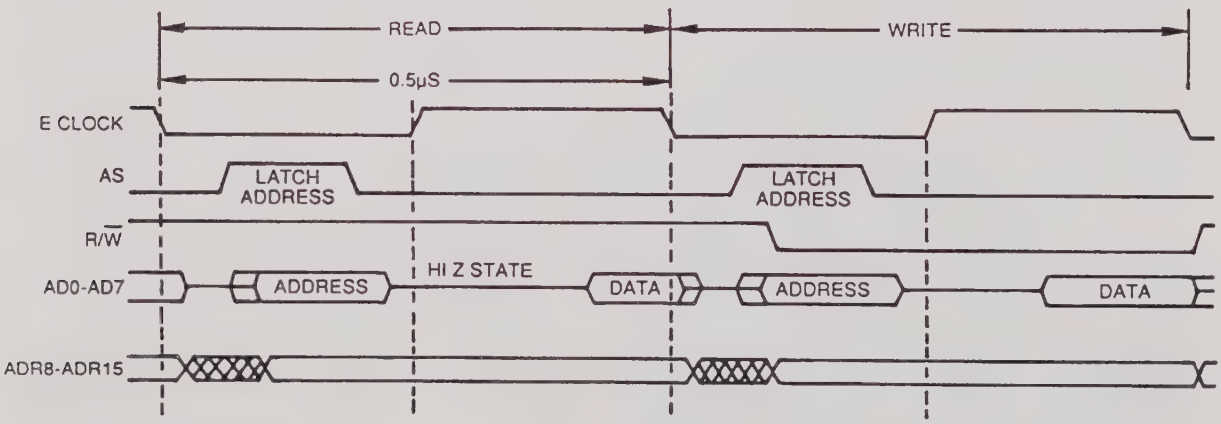


Figure 2-7. Microprocessor Timing Diagram.

Table 2-2 lists the names, pins and address range that will cause the respective outputs to go low.

Table 2-2. I/O Processor Board Memory Map

IC Pin Address Range (Hex)	Name	Source	Destination
0020-002F	DISPLAY	U4-18	Front Panel Board
0030-003F	KEYBD	U4-19	Front Panel Board
0050-005F	GPIB	U4-17	U3-3
2000-2FFF	RAM	U4-20	U5-20, 22
8000-BFFF	ROM 2	U4-22	U6-20

The clock input (E) to the PAL (U4-16) is used to qualify the five outputs. This means that none of the five outputs will be selected unless a valid address exists, and this only occurs when E is high. The R/W input (U4-23) is also qualified when E is high, and it appears at the output (U4-15) to drive the write enable (WE) of U5-27.

2.4.3.4 RAM (Schematic sheet 1, location 6B)

The microprocessor uses the random access read/write memory (U5) as a scratch pad and as a memory for stored settings. Although 15 address lines are applied for a possible 32K x 8 memory, only 8K x 8 is necessary. In detail, the data RAM memory stores the following material:

- Pending parameters/modes with operator/external requests execution.
- A listen buffer of all commands received from the External I/O bus.
- A SRQ buffer of defective commands from the External I/O bus.
- Display viewing angle and backlight setting.

The RAM (U5-20) is selected by the output of the address decoder (U4-20) which also enables the output (OE) internal three-state buffers.

2.4.3.5 ROM (Schematic sheet 1, location 4B)

The read only memory (U6) contains the initialization and monitor program for the 6803 microprocessor. This information includes:

- Menu's and menu trees.
- Numeric parameter limits.
- Operating mode restrictions.
- A list of External I/O commands for operator reference.
- Error messages.

2.4.3.6 Address Switch Read Buffer (Schematic sheet 1, location 4C)

An 8-section DIP switch on the rear panel is connected through the motherboard to U7 on the I/O Processor Board, and is used to select the IEEE-488 address for the model 869. The pull-up resistors in resistor pack RN2 ensure that an open switch causes the respective input lines (U7 — pins 2 through 9) to be pulled high, while a closed switch produces a low input. The 8 non-inverting tri-state buffers within U7 will pass the switch address onto the multiplexed address/data bus to be read into U3 (the IEEE-488 interface device) when U3 requests the address by enabling the address switch enable (ASE) line (from U3-4 to U7-19).

2.4.3.7 IEEE-488 Interface (Schematic sheet 1, location 2D)

The GPIA (U3) provides the means to interface between the IEEE-488 standard instrument bus and the 6803 microprocessor.

GPIA/MPU Interface lines — The GPIA is selected by the GPIB/ output (U4-17) of the address decoder which drives its chip select (U3 pin 3). The R/W input of the GPIA (U3-5) is driven directly from the MPU (U1-38). The address lines A0, A1, and A2 (U3-37, 38 and 39) are used to select the various registers within the GPIA, and the bi-directional data bus (U3-7 through 14) allows the transfer of data between the MPU and the GPIA. The reset input (U3-19) of the GPIA is activated by the master reset MR from the main microprocessor board.

When the external instrumentation controller sends either the instrument's talk or listen address or a serial poll, U3 signals the microprocessor by activating the interrupt request line, IRQ (U3-40). The 6803 can then interrogate any of the internal registers within U3, by sending out one of eight addresses to RS0, RS1 and RS2, and then data can be read from or written to one of the eight internal registers via the bi-directional data bus (DB0 through DB7).

The E (enable clock) from the 6803 is used by the GPIA to enable the address inputs (C5, RS0, RS1 and RS2) and the R/W input and to enable data transfer on the MPU data bus.

GPIA Interface lines — The GPIA provides a set of eighteen interface signal lines between the MPU and the IEEE-488 bus. The signal lines IB0-IB7 are bi-directional

lines for the 7-bit ASCII interface messages and device dependent messages. Three byte transfer handshake lines (DAC, RFD and DAV) allow for proper handshake of each data byte on the bus between sources and acceptors.

The attention (ATN), interface clear (IFC), service request (SRQ), remote enable (REN) and end of identify (EOI) lines are used to manage an orderly flow of information across the interface lines. The transmit/receive control signal T/R2 (U3-27) is used to control the transceivers on the motherboard which drive the interface bus.

The address switch enable (ASE) line (U3-4) controls the select line to the address switch read buffer (U7-19). The 6803 can read-in the contents of the switch by reading the contents of the address register in U3. This causes U3 to set ASE low during the E-clock (data) portion of the microprocessor clock cycle placing the 869 address on the data bus.

2.4.3.8 Beeper (Schematic sheet 2, location 2B)

To generate an audible beep, the 6803 generates a positive pulse at port 17 (U1-20) which drives the clear line (U14-11) to reset all the outputs of a 14-stage counter. The low's on Q13 and Q14 produce a high at the output of U9-8 which enables the 2 MHz clock (E) to pass through U9 pin 4 to 6 into the clock input of the counter (U14-10). Q10 produces an approximate 2 kHz (÷1024 output) square wave which drives the base of Q1. The transistor turns on and off, alternating the current through the beeper, LS1. The 2 kHz output of Q10 continues to produce a beep until Q13 and Q14 both go high which will disable U9, blocking the clock and consequently stopping the beep.

2.4.3.9 Isolated Serial Interface (Schematic sheet 2, location 5C)

The optically coupled isolators, U10 and U11, couple information between the I/O processor and main microprocessor board and isolates the instrumentation ground from the model 869 circuit ground. U10 sends two signals, front panel receive (FPRX) and clock (FPCLK), from the I/O Processor Board while U11 receives two signals from the main microprocessor board, the front panel transmit (FPTX) and system reset (SYSRST) signals.

2.4.3.10 Dial Encoder (Schematic sheet 2, location 2C)

The dial encoder is used to increment or decrement the selected parameters on the display. A Ø1 and Ø2 clock from the front panel board have a 90° phase relationship that determines the direction the dial has been turned while the number of pulses is used to determine the amount of rotation. The Ø1 signal drives the D input of U13B while the Ø2 supplies the Clock input, and Ø1 will either clock a high through to the Q (U13-9) indicating a clockwise rotation or a low indicating a counterclockwise rotation of the dial (see Figure 2-4). The DIREC output of U13-9 is fed to P12 (U1-15) of the microprocessor. The Ø1 and Ø2 signals are also used to produce a clock signal, KNOB, at the Q/ output of U13A which connects to the microprocessor at P20 (U1-8).

2.5 THE REFERENCE/CALIBRATOR BOARD (REF/CAL)

2.5.1 Function

The Reference/Calibrator Board serves to calibrate, test, and trigger as well as supply voltage and frequency references for the model 869. This board provides several resources to the signal modules as well as interfacing to the 68000 VME board. These resources include: a digital voltmeter (DVM) and frequency counter for calibration and diagnostics, an internal trigger source, a 10 MHz frequency reference, ±10V amplitude references, and a 16-bit DAC with a 16-channel sample and hold output. These resources are controlled by a local 6803 microprocessor that interfaces with the 68000 microprocessor on the VME board via a dual port RAM and local non-VME bus.

2.5.2 Block Diagram Description

Figure 2-8 shows the block diagram of the model 869's Reference Calibrator board. The 6803 microprocessor is the heart of the Reference/Calibrator board and is operated in its expanded multiplexed mode. The address and data latches serve to demultiplex the address and data information from the time multiplexed address/data bus (AD0-AD7). Also connected to the address/data bus is a 16k x 8 EPROM, a frequency counter and digital voltmeter (DVM) that are driven with signals and voltages from the modules via the calibration bus. A dual port RAM is also connected to the busses. The 6803 (Ref/Cal) and the 68000 (VME board via local bus) operate on two separate busses to exchange data through the dual port RAM without interfering with one another.

The address bus (A0-A7) from the 6803 is used to select the memory location desired in EPROM, drive the address decoder and data strobes, and to enable devices throughout the board.

The data bus (D0-D7) provides inputs to control latches, sample and hold latches, DAC latches, and the system trigger control. The system trigger control circuit receives the system trigger from the rear panel BNC and supplies four versions, which with an internally generated trigger derived from the 10 MHz oscillator, can be selected by the trigger select multiplexer. The selected trigger signal can drive both the output BNC (SYS TRIG OUT) and a line on the motherboard system timing bus. The 10 MHz oscillator output is also used as an internal reference for the reference select circuit. The 10 MHz reference signal and the selected trigger signal comprise the two lines of the system timing bus. The reference select circuit simply selects either an internal reference or an external reference from the 10 MHz REF IN BNC, and drives the output 10 MHz REF OUT BNC.

A 16-bit DAC converts the digital input from the DAC latches into an analog output that drives 16 sample and hold amplifiers, only one of which is enabled at a time by the sample and hold latches. A 16 sample and hold amplifier outputs form the DAC bus on the motherboard which provides 16 accurate, high resolution control voltages for use by the modules (2 lines/module) to control variable parameters. Positive and negative 10 volt references are generated on this board and applied to the motherboard power distribution bus while a +2V reference is used by the 12-bit ADC in the DVM circuit.

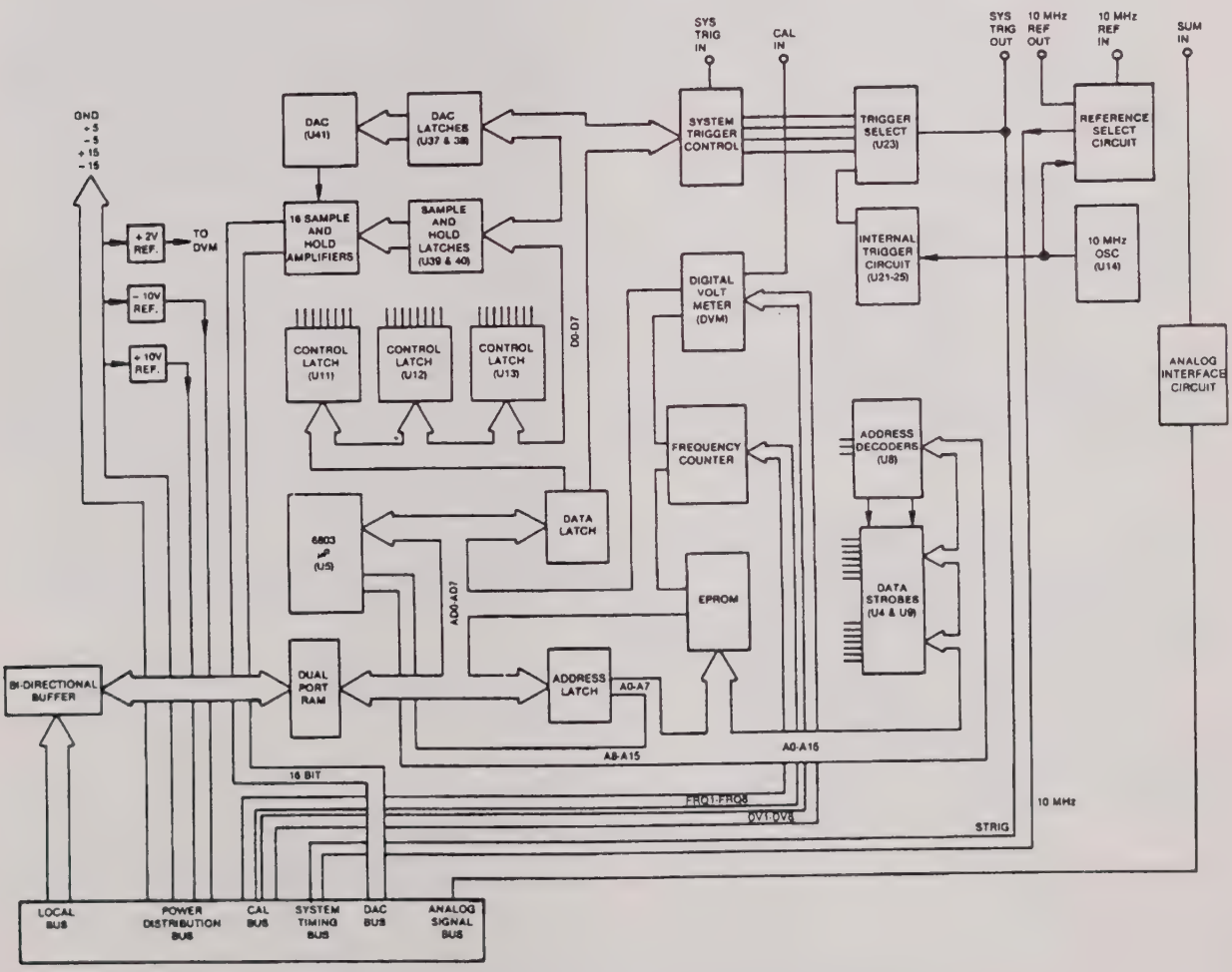


Figure 2-8. Reference Calibrator Board Block Diagram.

2.5.3 Circuit Description (Drawing Number 1104-00-3385)

2.5.3.1 Microprocessor (Schematic sheet 1, location 7C)

The 6803 microcomputer, with 128 bytes of internal RAM, is operated in its expanded multiplexed mode (mode 2).

In this mode: port 3 (P30-P37) functions as a time multiplexed address/data bus, port 4 (P40-P47) as the high byte of the address bus (A8-A15), and pins 38 and 39 are assigned as a read/write (R/W) and address strobe (AS) line. This operating mode is asserted at reset by the logic levels of P20, P21 and P22 which will be a low, high, low (binary 2) at reset (SYSRST 0) due to the diodes CR1, CR17 and the pull-up resistor R2.

A clock oscillator and divider circuit within the microprocessor uses an external 4 MHz crystal connected between XTAL1 and XTAL2 to generate a 1 MHz system enable (E) clock at U5-40.

2.5.3.2 Address and Data Latch (Schematic sheet 1, location 5C)

The address and data latches (U2 and U3 respectively) serve to demultiplex the address and data information from the time multiplexed address/data bus.

U2 is clocked by the address strobe line from the 6803 microprocessor when an address appears on the address/data bus. U3 is clocked by the system enable clock to latch data when it appears on the address/data bus.

2.5.3.3 EPROM Memory (Schematic sheet 1, location 7B)

The EPROM memory, U1, is addressed by 14 address lines (16k x 8) and contains the wake-up and monitor program for this board. The output enable line (U1-22) is driven by the system enable clock (E) from the microprocessor, which is buffered and inverted (BE) by the exclusive OR gate (U6-B). The chip is selected (CE at U1-20) when any address from $C000 to $FFFF appears on the address bus and is decoded by U8-B, which drives its ROM output (U8-9) low.

2.5.3.4 68000 Interface (Schematic sheet 1, location 5A)

The 6834 (U7) is a dual port memory unit which enables two processors, the Ref/Cal 6803 and the VME 68000, operating on two separate busses to exchange data without interfering with the devices on the other bus. It contains 256 bytes of dual port RAM which through decoding are found at addresses $B000 to $B3FF.

A local bus on the motherboard connects the 68000 to the dual port RAM via a bi-directional buffer, U10. The pins on the right hand side of U7 on the schematic are 68000 data address and control lines, while the left hand pins of U7 interface with the Ref/Cal's 6803. Communication is in either direction, and either processor can access the same memory location as separate address and data lines are available to each processor.

The sequence of events would occur as follows: the 68000 writes a command into U7 which signals the 6803 to read in the command and execute it. Conversely, the 6803 would write a command into U7, which would signal the 68000 to read in the command and execute it.

For example, commands from either the front panel (local) or the instrumentation controller (remote) are sent from the I/O processor to the 68000 VME board, and then communicated into the 6803 Ref/Cal processor via the dual port RAM, U7.

Table 2-3 lists the allocation of address within the dual port RAM, and shows the type of information being transferred between the Ref/Cal and VME board.

Table 2-3. Dual Port Ram Allocation

Info. Cat	Address	Name	Function
Trigger	B000	Trigger Control Register	Selects trigger mode (int, ext, event or time delay) and slope (+ or -).
	B001	External TriggerLevel Register	Selects level.
	B002-B005	Internal Trigger Frequency Reg.	Sets frequency.
	B006-B009	External Trigger Event Delay	32 bit binary integer
	B00A-B00D	External Trigger Delay Value	Sets delay time.
DVM	B010	DVM Input Control Register	Selects channel, range.
	B011	DVM Control Register	Sets mode and number of readings.
	B012, B013	DVM Read Register	Integer value (±4096) in millivolts.
	B016	DVM Settling Time Register	Time before a read is initiated.
Counter	B020	Counter Input Control Register	Selects channel, range, input polarity.
	B021	Counter Mode Control Register	Selects counter mode
	B022	Counter Rate Control Register	Sets gate time and period average.
	B023	Counter Time Out Register	Specifies maximum amount of time allowed for counter measurement.
	B024-B027	Counter Read Register	32-bit long integer value.
Sample	B030	Sample and Hold Mode Control	Selects sample time and number of channels.
	B032-B051	Sample and Hold DAC Values	The 16 sample and hold amplifier values.
Temp.	B058-B059	Temperature Read Register	Integer value, 10mV = 1°C.
Interface Controls	B060	Execute Register	Tells Ref/Cal processor to examine parameter in Ref/Cal for value changes and update.
	B061	Self-Test Register	Instructs Ref/Cal processor to perform Self-test.
	B062	External Ref. Control/Status Reg.	Sets reference to int. or ext. and detects if ext. input is present.
	B063	Temperature Alarm Register	Sets alarm temperature for Ref/Cal board.
	B064	Internal Status Register	This register explains the cause of an interrupt.
	B065	Interrupt Mask Register, Wake-Up Register	Sets interrupt masking. When power is turned on, the Ref/Cal initializes itself, writes $SS in the register, and then waits for the 68000 to finish its initialization and write $AA into this register. This process ensures synchronization between the 6803 and 68000.

2.5.3.5 Address Decoder (Schematic sheet 1, location 3D)

The address decoder, U8, is a dual 2-line to 4-line decoder demultiplexer. The B section of U8 decodes address lines A14 and A15 creating four 16k zones, as in Table 2-4.

Table 2-4. 16k Zone Address Decoder

U8 Pin	Zone	Address Range	Size	Enables
12-Y0	0	0000-3FFF	16k	U8A decoder via U58A
11-Y1	1	4000-7FFF	16k	—
10-Y2	2	8000-BFFF	16k	RAM (U7)
9-Y3	3	C000-FFFF	16k	ROM (U1)

The Y0 (Zone 0) of U8 is inverted by U58A and used to enable U8A which will subdivide the address range of Zone 0 (0000-03FF) into 4k zones by decoding the A5 and A6 address lines, as in Table 2-5.

Table 2-5. 4k Zone Address Decoder

U8 Pin	Zone	Size	Name	Enables
4-Y0	0	4k		
5-Y1	1	4k	CTR	(U33) Counter
6-Y2	2	4k	REGS1	(U4) data strobe
7-Y3	3	4k	REGS2	(U9) data strobe

2.5.3.6 Control Data Strobe (Schematic sheet 1, location 4B)

As shown in the above table, U8A decoder is used to select either U4 or U9 with an active low at G2B pin 5. U4 and U9 are also decoders and enable the following devices through the Ref/Cal board, as seen in table 2-6.

2.5.3.7 Control Latches (Schematic sheet 1, location 1A)

The decoder U9 pins 11, 10 and 9 are used to enable the three control latches, U11, U12, and U13, that can be used to latch data off the data bus and drive the following, as seen in table 2-7.

The function of each of these lines will be discussed in more detail in their respective circuit descriptions.

2.5.3.8 Internal/External Reference Circuit (Schematic sheet 2, location 3-8D)

The external 10 MHz rear-panel BNC reference in (Ref In), and internally generated 10 MHz from oscillator U14 are applied to separate comparators U15A and U15B. The external reference, if present, is ac coupled through C23 and R6 and applied to IN1A. The other input of the comparator, IN1B, has a reference voltage applied, developed by R5 and R7. As long as a valid reference exceeds the reference voltage it will appear at the output of the A comparator. The REFCLK out of U15-4 is applied to U16-4 (the D0 input of a 1 of 8 multiplexer). The internally generated 10 MHz from U14 (a temperature compensated crystal oscillator — TCXO) is processed by the lower B comparator in much the same way as the external reference, in that R9 and R10 set up a reference on IN2A and the clock is applied to IN2B. The processed clock out of the comparator is enabled or disabled by the output reference select line (REFSEL) from port 1 (P13) of the 6803 microprocessor. The 6803 has an input control line (EXTREF) that is used to sense whether an external reference signal is present (U5-14). This signal is true if an external REFCLK is present, charging C18 and turning on Q1, supplying a logic zero to U5-14.

Table 2-6. Decoders U4 and U9

Decoder U4			Decoder U9		
Pin	**Name**	**Enables**	**Pin**	**Name**	**Enables**
Y0-15	DACHI	(U37)DAC	Y0-15	ROSTB	(U26) Trigger Control DAC
Y1-14	DACLO	(U38) HI & LO bytes	Y1-14	RISTB	(U21) Internal trigger counter
Y2-13	SH1	(U39) Sample	Y2-13	R2STB	(U36) DVM
Y3-12	SH2	(U40) Hold	Y2-12	R3STB	(U36) DVM
Y4-11	DNC1	(U6D-DNCE1) (U18) Delay Counter	Y4-11	R4STB	(U12) Control latch
Y5-10	DNC2	(U54) Trigger	Y5-10	R5STB	(U13) Control latches
Y6-9	DNCK1	(U18) Delay Counter	Y6-9	R6STB	(U11) Control latches

Table 2-7 Control Latch Enables

	U11		U12		U13	
Pins	Name	Drives	Name	Drives	Name	Drives
19 18 17	CTRCH0 CTRCH1 CTRCH2	(U30) Frequency Counter Channel Select	INTR0 INTR1 INTR2	(U25) Internal Trigger	DVMCH0 DMVCH1 DMVCH2	(U34) DVM Channel Select
16 15 14	CTRCH3 CTRCH4 CTRCH5	(U32) Frequency Counter Multiplexer	INTR3 INTR4 TRIG1	(U32) Run/Hold	ITRON DVMRUN	(U24) VCO on/off (U36)
13	TRGSLP	(U6C) Trigger Slope	TRIG2 TRIG3	Trigger Select	DMVCH3 DVMCH4	(U35) DVM Multiplexer
12	TRGMODE	(U54) Trigger Mode			DVMCH5	

The 1 of 8 multiplexer, U16, will switch through to the output (U16-5 and 6) either the D0 input (external reference) or D1 input (internal reference) depending on the REFSEL line input control (U16-11). The Y output of U16 drives U20A which translates the TTL 10 MHz to an ECL compatible 10 MHz and 10 MHz/, which is then applied to the motherboard system timing bus. The W output of the multiplexer (U16-6) is the input to the Q2/Q3 circuit which buffers the selected 10 MHz clock and drives the output BNC J101. C24/C25 are speed-up capacitors to couple the input signal to the transistors, and Schottky diodes CR3/CR4 prevent storage delays that would result from allowing the transistors to go into heavy saturation. The 50Ω output impedance for REF OUT is provided by R19/R20.

2.5.3.9 Trigger Control (Schematic sheet 2, location 1-8A)

The system trigger is applied to the model 869 rear panel BNC J102 and is limited to 5 and -5 volts by CR5 and CR6 before being applied into IN1A of the dual comparator U17. The other input to the A comparator (IN1B) is derived from U26, an 8-bit DAC which functions as a programmable trigger level controller under control of the data bus lines D0-D7. Through software control the threshold level produced by the DAC can be controlled, and input signals crossing the selected threshold will be conditioned and passed to U6-9. The exclusive OR gate U6C acts as a controlled inverter driven by data latch U11-13 to produce either a positive or negative going trigger (slope). R45 provies a small amount of positive feedback (hysteresis) for noise imunity. The EXTTRIG is fed into the trigger select multiplexer (U23-4), into 1A and 2B of the quad 2 to 1 multiplexer (U54-2 and 6), and into comparator U17B. When an EXT trigger is present, it will gate the U17B circuit into oscillation, the 10 MOSC signal, as seen in the simplified circuit figure 2-9. The following descriptions refer to the schematic and to figure 2-9.

Serial loaded ASIC counter U18 is a synchronous 36-bit divide by N down counter used to produce both the delayed (mode A) and divided (mode B) trigger. The number "N" is shifted into the SDIN input with each positive SCLK transition. After last data bit of the 36-bit value has been shifted in, SEN (enable) transfers the contents of the internal shift register into internal latches. This value will determine the amount the EXTRIG will be delayed or divided by. When operated in mode A (delayed trigger) the EXTRIG is fed to the load inputs of U18, and the 10 MOSC drives the clock (U18-4, 9) producing (100 ns) delay periods. For example, if a divide by 10 is loaded into U18 the external trigger will be delayed by 10 clock inputs (10 x 100 ns or 1 ms) before it appears at U18 CYA and finally drives the trigger select multiplexer, U23 pin 3. U19 terminates the delay if the external signal goes false, gating 10 MOSC off, before the delay count is complete.

When the divided trigger mode (B) is selected (U54-1 is high), the external trigger signal clocks U18, where it will be divided down by 'N' and then appear out of CYA and at the input of the trigger select multiplexer, U23 pin 14.

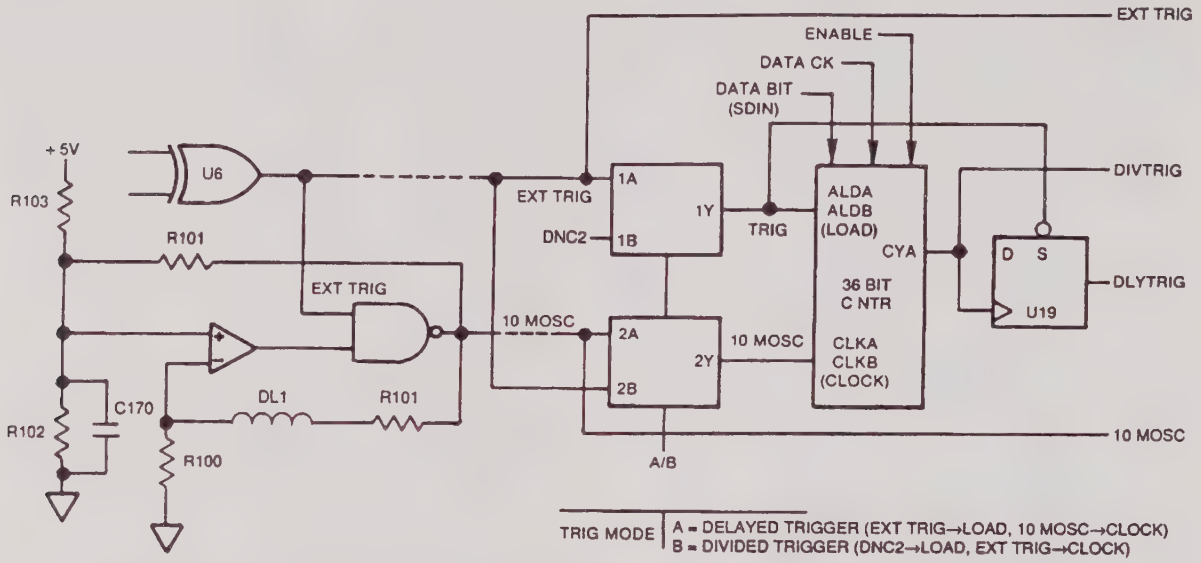


Figure 2-9. Trigger Control Gateable Oscillator

2.5.3.10 Internal Trigger (Schematic sheet 5)

The internal trigger frequency is generated by a phase locked loop synthesizer comprised of U21, U22, U24 and U25. Figure 2-10 illustrates a block diagram of this circuit. U21 has a +R section that has been permanently set up by RA0, 1 and 2 to divide the 10 MCLK input (U21-17) by 4096 to produce a 1.22 kHz reference to the internal phase detector. The other internal divider (+N) is serially loaded with a 14-bit value (U21-10, 11 and 12) and will divide the 5 to 10 MHz VCO's output by any value between 4096 to 8192. For example, if the +N counter was initialized with 4096, the 5 MHz output from the VCO will produce 1.22 kHz into both inputs of U21's internal phase detector. The Phase Detector outputs error pulses (U21-6) which are integrated and filtered to produce a dc error voltage which will maintain the VCO's output at 5 MHz. If the division ratio is increased within U21's +N counter from minimum (4096) to maximum (8192) the error voltage into the VCO will cause the output frequency to increase to 10 MHz. This will return both inputs to the phase detector to be 1.22 kHz and lock the loop. The VCO 5 to 10 MHz output (INTTRIG1) is fed into both the trigger select multiplexer U23-1 and U25, a 5-bit programmable divide by 2^N counter. The value of "N" loaded into U25 can be anywhere between 1 to 31 and through software control a larger range of lower INTTRIG frequencies can be obtained.

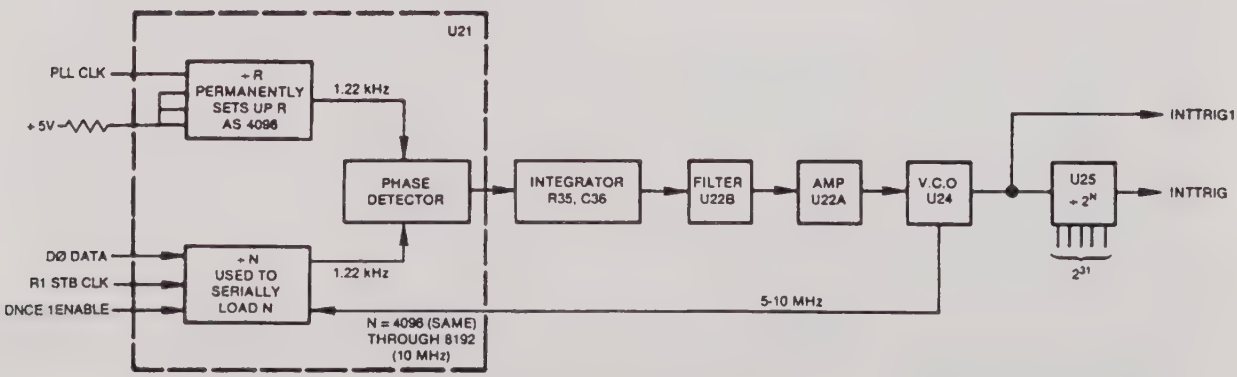


Figure 2-10. Internal Trigger Circuit

2.5.3.11 Trigger Select (Schematic sheet 2, location 2C)

The 1 of 8 multiplexer, U23, is permanently enabled and controlled by TRIG1, 2 and 3 from control latch U12, to switch one of the 8 different forms of trigger through to the outputs Y and W. The output system trigger (STRIG) is converted from TTL to ECL by U60 before being applied onto the motherboard system timing bus. The W output TRIGMEAS of U23-6 is fed into another multiplexer, U32, and if selected will be applied into the frequency counter U33 to determine trigger frequency. U23 inputs D6 (5V) and D7 (0V) are used when a manual trigger is desired. The INTTRG1 (5-10 MHz) is fed into U19B to provide a divided by 2 version, INTTRG2 (2.5-5 MHz), which is also available on the input of the trigger select multiplexer (U23-15).

The STRIG on the motherboard system timing bus is also buffered and supplied to the model 869 rear panel BNC J103 as seen in schematic sheet 3, location 1-8 CD.

2.5.3.12 DVM and Gain Select (Schematic sheet 4, location 1-8CD)

A dedicated signal line from each of the 8 module slots (2 available per each 680-03) is connected via the motherboard calibration bus into the Ref/Cal Board DVM for the purpose of calibration and diagnostics. Figure 2-11 illustrates a block diagram of the DVM and gain select circuit.

The first analog multiplexer U34, under the control DVMCH0, DVMCH1 and DVMCH2 from control latch U13, will select one of the eight inputs from each of the modules. The selected output is buffered by U52 and then applied to another analog multiplexer U35-4 (X1). This output is also attenuated by 4 (RN4) and then fed as a separate input to U35-5 (X4). Three other inputs are applied to the analog multiplexer U35: DVCO from the motherboard, CAL IN from the rear panel BNC J104 (where a known voltage can be applied to verify correct operation of the DVM), and a temperature input voltage (U35-12). The temperature input from the semiconductor temperature sensor CR9 gives a +10 mV change per degree celsius. This temperature indication signal is also fed to the motherboard via amplifier U52B, as an input to the modules.

The analog multiplexer U35, is controlled by DVMCH3, DVMCH4 and DVMCH5 to switch one of its five inputs through to the output and to the DVM IC U36.

U36 is a 12-bit plus sign integrating A/D converter, that converts the analog voltage on pin 35 into an equivalent 12-bit digital word which is passed to the 6803 microprocessor, via the address/data bus lines AD0-AD7.

Each of the buses are those called out in the 68000 VME schematic diagram and the Main Interconnect schematic diagram.

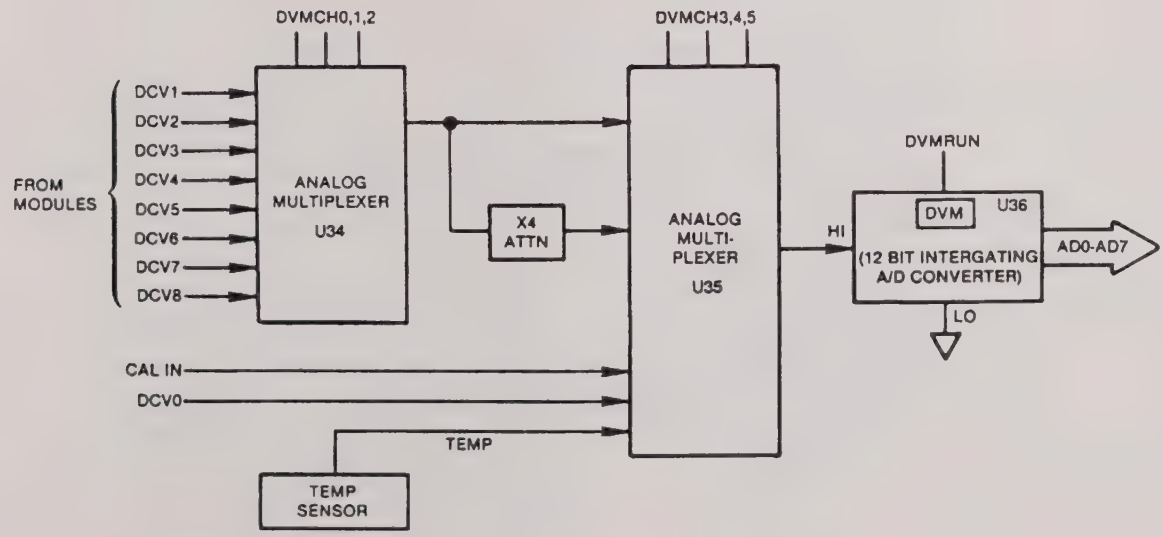


Figure 2-11. DVM and Gain Select Block Diagram

2.5.3.13 Frequency Counter and Select
(Schematic sheet 4, location 2-8B)

A dedicated signal line (FRQ1-FRQ8) from each of the module slots is, like the DVM circuit, fed into multiplexer U30, where one will be selected by control lines (CTRCH0-CTRCH2) and passed to the output at U30-5. This output is directly fed to another digital multiplexer, U32-4, and indirectly fed to U32 via a +20 circuit (U31). U32, under the control of (CTRCH3-CTRCH2) will switch one of its seven inputs to the output and into U33 to be counted.

Figure 2-12 illustrates a block diagram of the frequency counter. If an internal trigger of a known frequency is selected, the multiplexer U32 can switch TRIGMEAS to the input of the counter and verify that the counter reading matches the set internal trigger frequency. The other inputs, 10 MOSC, 10 MCLK, REFCLK, and OV-MOSC can also be fed through and counted by U33 to verify the signals are both present and accurate.

2.5.3.14 +10V, -10V and +2V Reference
(Schematic sheet 4, location 1-8A)

The +10 and -10V references are generated by U50, U51 and then buffered by U29, Q4, and Q5 before being applied to the motherboard power distribution bus. Among other things, the +10V from Q4 is divided down by RN2 and R63 (adjustment) to +2.048V. This voltage is used by the 12-bit analog to digital converter (U36, DVM IC).

2.5.3.15 Sample and Holds (Schematic sheets 6 and 7)

A DAC is sequentially programmed with 16 digital values (from stored calibration constants), generating a series of 16 variable analog voltage levels. Each of these levels is, through digital control, latched into any one of the 16 sample and hold amplifiers. The outputs of the 16 amplifiers are then 16 separate, programmable dc voltages. This 16-channel output forms the DAC bus on the motherboard and is used to provide 16 accurate, high resolution control voltages for use by the modules (2 lines/module slot) to control variable analog parameters. Figure 2-13 illustrates a block of the DAC, latches and sample and holds.

The 16-bit resolution DAC, U41, is driven by a 16-bit word from data registers U37 and U38 that latch the two 8-bit words from the data bus D0-D7. U39 and U40 are also driven by the 8-bit data bus, D0 through D7, and their 16 output lines are used to sequentially latch the DAC output to the sixteen sample and hold amplifiers. The selected sample and hold will, when selected, accurately duplicate and buffer the current analog volt-

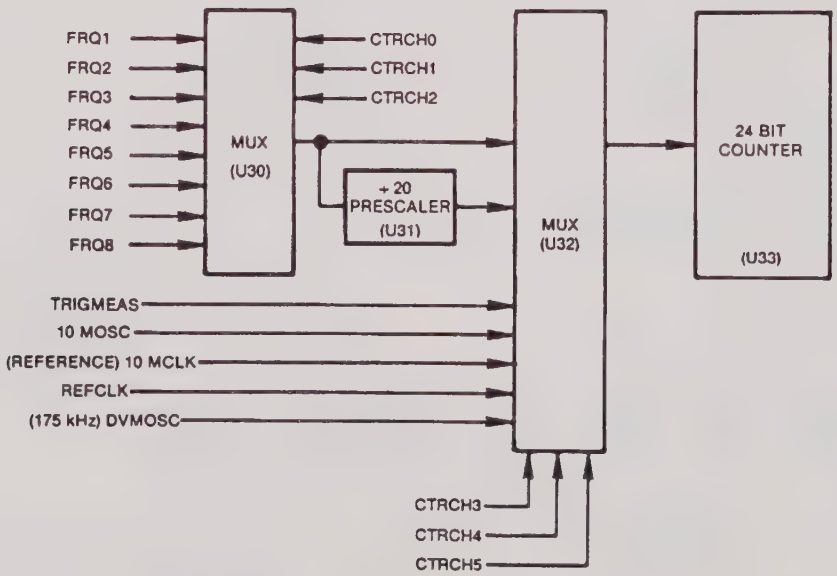


Figure 2-12. Counter Logic Diagram

age being produced by the DAC, U41. Since all the sample and hold amplifiers are the same, refer to sample and hold amplifier 7 (schematic location 64D). U39 will select this S&H amplifier by placing a logical 1 on U39-19, which will switch comparator U42A and turn on Q6, allowing the currently produced analog voltage from U41-19 to pass through Q6 and charge C96. The voltage from the DAC, and therefore the voltage on the sample and hold capacitor (C96) is buffered by U43A and drives the module via the motherboard DAC bus. The filter arrangement made up of the two resistors (within RN5) and C112 is present to filter the spikes produced when the comparator U42 switches from off (-10V output) to on (+15V). When Q6 is off, C112 is isolated from the DAC output, and retains its charge until the next refresh cycle.

2.5.3.16 Analog Sum In (Schematic sheet 3, location 4-7AB)

The analog sum interface will allow a signal delivered to the rear panel BNC J105 to be placed onto the motherboard analog sum bus and summed into any of the eight plug-in signal modules. Any module which may support summing capability may either disconnect from, drive, or receive the analog information. This summing allows two or more signals to be summed to create composite waveforms on any channel. This capability is not supported by the 680-03 pulse generator module or by the model 869.

2.6 VME MICROPROCESSOR BOARD

This section describes what the VME Microprocessor board does, how it interfaces with other signals on the Main Interconnect board, describes the VME Microprocessor board block diagram, and how the VME Microprocessor board circuits work.

2.6.1 Function

The VME Microprocessor board:

1. Asserts a system-wide reset at power-up which initializes the operating state of the entire model 869.
2. Identifies each function module and postion, executes instructions located in function module read only memory via the System Mainframe VME bus, and controls the operating state of all function modules.
3. Initializes the real time clock and manages all timekeeping functions.
4. Monitors and logs minimum and maximum cabinet temperature excursions.

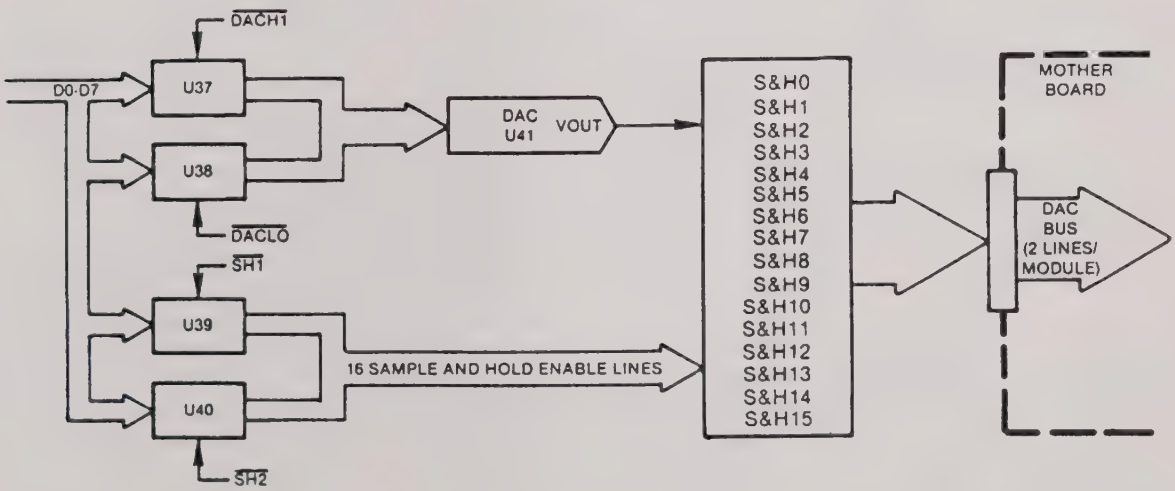


Figure 2-13. Sample and Hold Circuit

5. Receives front panel control inputs and External I/O commands from the I/O Processor Board.
6. Sends Status messages to the I/O processor for front panel display and for control of the External I/O Bus.
7. Supervises Ref/Cal Board operation.
8. Runs the complete Self-test procedure.
9. Retains calibration auto-correction factors, stored settings, time, temperature, and date data in its non-volatile static RAM.
10. Sums the model 869 rear panel System Sync In input signal to the model 869 System Sync (SSYNC) bus. Also buffers the System Sync (SSYNC) signal and applies it to the model 869 rear panel System Sync Out output BNC.
11. Operates the DFI relay contacts.

2.6.2 Interface with the Main Interconnect Buses

This section describes the functions of the signal lines in each of the Main Interconnect Buses that interface with the VME Microprocessor board. Figure 2-14 shows the buses on the Main Interconnect board that interface with the VME Microprocessor board; the signal names in

2.6.2.1 VME Bus

The VME bus is the communication path between the VME Microprocessor board and the function modules. The status of any of the function modules is communicated to the VME Microprocessor board over this bus; instructions located in function module memory are fetched and executed over this bus. This bus is also the communication path for status signals provided by the function modules.

The VME bus in the model 869 follows the single level arbitration standard called for in the VME bus Specification Rev C.1 published by Motorola Inc. Refer to this

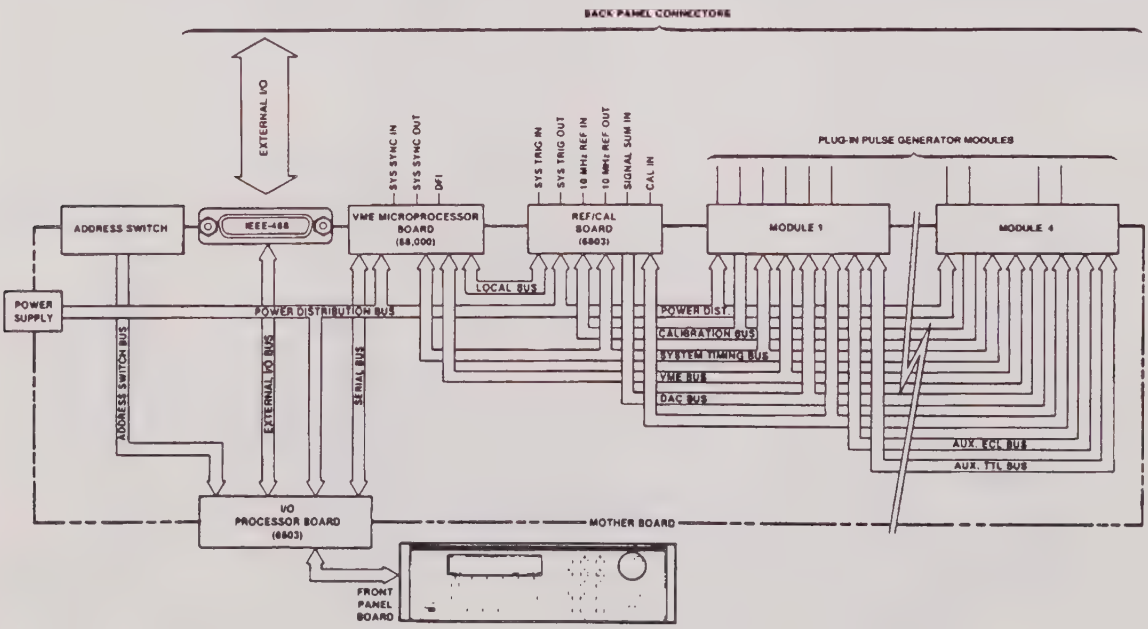


Figure 2-14. VME Microprocessor Board Bus Interface

specification for information about the function and timing of the VME Bus signals.

Table 2-8 lists the VME Bus signals not used by the VME Microprocessor board in the model 869.

Table 2-8. VME Signal Exceptions

VME Bus Spec.	Name(s)	VMEμP Pin(s)	VME Connector
7.61	LWORD	P27/C13	J1/P1
7.6.1	+12V	P27/C31	J1/P1
7.6.1	BCLR	P27/B2	J1/P1
7.6.1	ACFAIL	P27/B3	J1/P1
7.6.1	BG3IN	P27/B10	J1/P1
7.6.1	BRO	P27/B12	J1/P1
7.6.1	BR1	P27/P13	J1/Pi
76.1	BR2	P27/Bi4	J1/P1
7.6.1	SERCLK	P27/B21	J1/P1
7.6.1	SERDAT	P27/B22	J1/P1
7.6.1	GND	P27/A17	J1/P1
7.6.1	IACKIN	P27/A21	J1/P1
7.6.1	-12V	P27/A31	J1/P1
7.6.1	+5V,GND	P28/B1	
7.6.1		thru	J2/P2
		B32	
	RESERVED, A24 thru I A31, and D16 thru D31		

2.6.2.2 Local Bus

The Local Bus connects only between the VME Microprocessor Board and the Ref Cal Board. It contains the LD0 through LD7 data lines, the LA1 through LA9 address lines, and the four signal lines LE (Local Enable).

LR/W (Local Read/Write), interrupt line AV2/ from the Ref Cal module dual port RAM, and CSRC/ (Ref Cal Chip Select) line. The VME board communicates with the Ref Cal Board by sharing data in a dual port RAM on the RefCal Board. Information about Ref Cal status is read from the Ref Cal board via this bus and control of Ref Cal board operation is asserted by writes to the Ref Cal board via this bus.

2.6.2.3 Serial Bus

The Serial Bus connects only to the I/O Processor Board. It contains two output lines called FPTX (Front Panel Transmit) and FPRST (Front Panel Reset) and two input lines called FPRX (Front Panel Receive) and FPCLK (Front Panel Clock).

The VME Microprocessor output lines FPTX (Front Panel Transmit) and FPRST (Front Panel Reset) drive optocouplers on the I/O processor board. The VME board controls the operation of the I/O board by generating serial commands on the FPTX (Front Panel Transmit) line. The VME board brings the I/O processor board to its power up state by asserting a reset signal on the FPRST/ (Front Panel Reset) line.

The two VME Microprocessor input lines FPRX (Front panel Receive) and FPCLK (Front Panel Clock) come from optocoupler outputs on the I/O Processor board. They pass serial data to the VME processor via a UART; the VME Microprocessor board monitors operation of the Front Panel and the GPIB bus by processing the serial data on this line.

2.6.2.4 System Timing Bus

The VME Microprocessor board connects only to the System Sync (SSYNC) line of the System Timing bus. This signal line is bi-directional; digital signals appearing on the System Sync (SSYNC) line are buffered for output at the rear panel Sys Sync Out BNC connector and signals appearing at the rear panel Sys Sync In input BNC connector are buffered and generated to the System Sync (SSYNC) line.

2.6.2.5 Power Distribution Bus

The VME Board gets all of its operating power from this bus. +5 Volts, +5 Volts Standby, circuit ground, and ±12 Volts are connected to the VME connector P27 per the VME bus Specification Rev C.1. ±15 Volts and -2 Volts are connected to the user defined pins of the VME connector P28.

2.6.3 Block Diagram Description

The VME Microprocessor board block diagram is provided as Figure 2-15.

2.6.3.1 68000 CPU

The 68000 CPU:

1. Executes instructions located in on-board ROM to implement all model 869 System Mainframe functions.
2. Executes instructions located in off-board ROM locations (i.e., ROMs on the function modules) to control operation of each respective function module.
3. Generates address and data on the LA1 through LA23 and LDO through LD1 5 lines which connect

locally to all on-board memory and peripherals and also latch to the VME Bus via the VME Latch under control of the VME Arbitration PALs.

4. Interfaces with interrupt priority circuits to detect on or off-board interrupts, determines the priority of the asserted interrupt, responds with an interrupt acknowledge value of 111 (Base 2) on the FC0 through FC2 lines, and processes the interrupt request. Detection of a 111 (Base 2) on the FC0 through FC2 lines is decoded by the Address Decoding circuitry which responds with the LIACK/ (Local Interrupt Acknowledge) Signal.

5. Responds to signals from the VME Bus arbitration control and VME Latch to manage the transfer of data over the VME bus.

6. Connects directly to the model 869 Local Bus for control of the Ref Cal Board.

7. Executes instructions that control the on-board Real Time Clock, DFI watchdog timer, and System Sync Interface circuits.

8. Generates the address and data strobe signals LR/ W, LAS, LU DS, LLDS and monitors the Data CPU (DTCPU) signal from the DTACK (Data Acknowledge) PAL to asynchronously transfer 16-bit data.

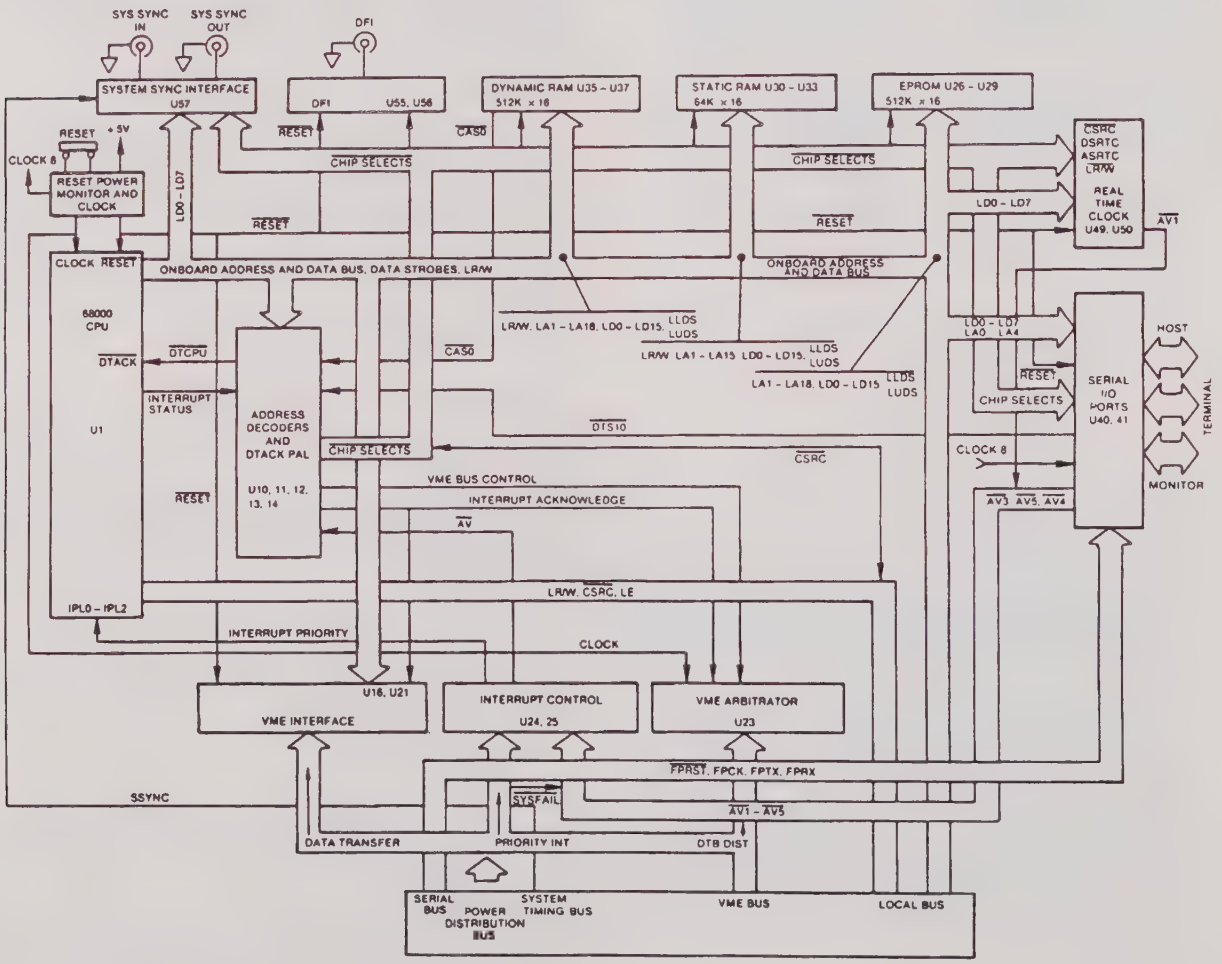


Figure 2-15. VME Microprocessor Board Block Diagram

9. Generates the VMA and LE strobe signals and monitors the VPA signal to synchronously transfer eight bit data to MC 8690 peripherals.
10. Monitors the BERR signal and performs exception processing when bus errors occur.
11. Monitors the RESET and HALT signal lines for reset conditions and resets the model 869 System parameters when asserted.

2.6.3.2 Reset and Power Monitor Control

Whenever a reset signal is asserted by this circuit, the model 869 assumes initial power-on conditions.

Two events cause the RESET and HALT signals to be asserted:

1. The +5V from the System Power Distribution bus is out of tolerance.
2. The VME Microprocessor Reset Switch has been pressed.

2.6.3.3 Interrupt Control

The Interrupt Control circuit detects:

1. On-board interrupts AV1 thru AV6.
2. Off-board interrupt signals IRQ1 thru IRQ7 from the VME bus.
3. The VME signal SYSFAIL.

The on-board interrupts and SYSFAIL have priority over the off-board interrupts IRQ1 thru IRQ7.

This circuit decodes the priority level of these interrupt signals and generates a binary code of this priority to the 68000 CPU on the signal lines IPL0 through IPL2. The signal AV is generated to the address decoder by this circuit whenever any of the on-board interrupts or SYSFAIL is asserted; this causes the Address Decoder to respond with the VPA signal which causes the 68000 CPU to respond with an auto-vectored interrupt acknowledge cycle.

Detection of an off-board interrupt (IRQ1 thru IRQ7) causes the Address Decoder to respond with the Local Interrupt Acknowledge (LIACK) signal which causes the 68000 CPU to respond with a vectored interrupt acknowledge cycle.

Either interrupt acknowledge cycle will cause the 68000 CPU to assert all 1's on signal lines FC0 thru FC2; this causes U9 to assert FC to the Address Decoder. When asserted, Address Decoder chip select generation is inhibited.

2.6.3.4 VME Interface Arbitration and Latches

The VME Bus Arbitration Control monitors the VME Bus Request (BR3), the Bus Busy (BBSY), Valid Peripheral Address (VPA), Off-board Address Detect (OFFBD), Local Interrupt Acknowledge (LIACK), and Local Address Strobe (LAS) signals.

Monitoring these signals allows the Arbitration Control to retain control of the VME bus unless an on-board access is detected by the 68000 CPU.

The VME latches are controlled by the BGBD signal generated by the Bus Arbitration PAL.

2.6.3.5 Address Decoders and DTACK PAL

The Address Decoder PALs and latches:

1. Decode the VMA, LE, LAS, LR/W and local address lines LA12 thru LA20 to generate the Strobe and Timing signals for selection and data transfer to the Real Time Clock and the Ref/Cal board (via the 869 Local Bus); also responds to the 68000 CPU and the VME Bus Arbitration Control PAL with the VPA signal.
2. Provide the LIACK and VPA signals to the VME Bus Arbitration circuitry during vectored interrupt acknowledge cycles.
3. Decode the Local Address lines LA1 thru LA23 for generation of I/O chip selects, DFI and System Sync control selects, DRAM, SRAM, and PROM chip selects.

The DTACK PAL:

1. Decodes all on-board 16-bit chip selects, the I/O port Data Transfer (DTSIO), and the dynamic RAM CSO signal and generates the DTCPU signal (data transfer to CPU) to the 68000 CPU (68000 CPU, 'DTACK' input) thus completing the Asynchronous Data Transfer Timing Cycle.
2. Monitors the VME bus DTACK signal when asynchronous data transfers are made over the VME bus. Should a device not respond in time, ASBERR will assert with the local address strobe (LAS). ASBERR is an input to a shift register clocked at 2 MHz. If the DTACK PAL doesn't detect the DTACK response on the VME bus by the time the ASBERR signal is shifted out, the signal Bus Error (BERR/) asserts. The 68000 CPU will respond by beginning exception processing that recognizes that the addressed peripheral doesn't exist.

2.6.3.6 Dynamic RAM

The Dynamic RAM occupies 512K of address spaces at the addresses 00000H thru 07FFFFH.

The dynamic RAM refresh and local bus interface signals are generated by an integrated Dynamic RAM controller chip.

There is no battery backup of the Dynamic RAMs. Loss of the +5V Supply from the Main Interconnect Power Distribution bus results in loss of any data stored in the dynamic RAMs.

2.6.3.7 Non-volatile Static RAM

The Static RAM occupies 64K of address spaces at the addresses 100000H thru 11FFFFH.

Backup batteries are part of the static RAM integrated circuit packages. Because of this the static RAMs retain data even though the model 869 System Power Bus is deenergized. Data retention is guaranteed for eight years from date of battery manufacture.

The static RAM retains stored settings, auto-cal parameters, and time and temperature data for the event logging functions.

2.6.3.8 EPROM

The EPROMs occupy 512K of address spaces at the addresses 080000H thru 0BFFFFH.

Locations 080000H thru 0BFFFFH contain the model 869 System Firmware; these instructions implement the model 869 System Mainframe multi-tasking functions.

Locations 0C0000H thru 0DFFFFH contain the model 869 System Library Firmware; these instructions are called for time to time by the model 869 System Firmware.

The chip select signal CSROMOH selects the lower 256K (addresses 080000H thru 0BFFFFH); CSROM1 selects the remaining locations which contain the model 869 system Library Firmware.

2.6.3.9 Real-Time Clock

The Real Time Clock maintains the current time of day and the current calendar date and operates from a backup battery supply (+5VSBY) when the model 869 is turned off and from the Power Distribution Bus +5V supply when the model 869 is turned on. The Real Time Clock always operates regardless of the condition of the model 869 power switch.

The Real Time Clock time base is the 32.768 kHz crystal oscillator circuit and is independent of any model 869 System Mainframe timing signal.

Data transfer to and from the Real Time Clock takes place via a multiplexed address and data latch connected to the Local Data LDO thru LD7 bus lines. The Address Decoder provides the Address and Data Strobes (ASRTC and DSRTC), the chip select CSRTC, and Local Read Write control LR/W.

When performing time and date logging functions, the 68000 CPU reads from the Real Time Clock registers the current value for the time and date.

2.6.3.10 Serial I/O Ports

The serial I/O ports consist of 2 dual Universal Asynchronous Receiver Transmitters U40 and U41 . Operation of the serial I/O ports is selected when the Address Decoder asserts either CSSIO1 or CSSIO2.

The Port Controller generates a 3.6864 MHz clock which is a baud rate clock for the Terminal, Host, and Monitor ports. This clock should always appear at TP41.

The I/O Processor board clocks the Front Panel Clock (FPCLK) line at 125 kHz; this signal appears at TP4-0. Data received on the Front Panel Receive (FPRX) line comes from the I/O Processor board and is synchronized with the Front Panel Clock (FPCLK) line. Serial data is transmitted from the I/O controller to the I/O Processor board via the Front Panel Transmit (FPTX) line.

After the RESET signal is asserted, the Serial I/O Port controller ICs are initialized by the 68000 CPU to the correct operating modes. Also, the RESET signal is buffered and sent via the model 869 Serial Interface Bus to the I/O Processor board on a signal line called Front Panel Reset (FPRST).

The Data Transfer Signal I/O (DTSIO) is asserted by the I/O port controller for the DTACK PAL to signify a successful data transfer to or from the 68000 CPU.

The Auto-vector interrupt 5 (AV5) is asserted by the I/O controller when the controller has received data from the I/O processor; the 68000 CPU responds to this with an auto-vectored interrupt acknowledge cycle.

The Monitor port interrupt is asserted with AV4; the Terminal and Host port interrupts are asserted on AV5.

2.6.3.11 System Sync Interface

A write by the 68000 CPU to location 0F5000H controls the System Sync In input selection. When the LD0 bit of the Local Data Bus is 0, the transfer of the signal at the

Sys Sync In input BNC to the model 869 System Sync (SSYNC) bus is inhibited; if LD0 is written as a 1 , the Sys Sync In signal is buffered to the System Sync (SSYNC) bus.

2.6.3.12 Discrete Fault Indication (DFI)

The DFI relay contacts close when:

1. The model 869 power is off.
2. A 68000 CPU failure occurs.

The DFI relay contacts close when the CSDFI signal is not regularly asserted. During the course of normal program execution, the 68000 CPU periodically asserts the address for the CSDFI. When selected, the watchdog timer is reset; the CPU must again assert the address for CSDFI before the watchdog timer times out.

The contacts will open whenever RESET is asserted and should remain open after release unless there is still a 68000 CPU problem.

2.6.4 Circuit Description (Drawing Number 1104-00-3226)

2.6.4.1 CPU Clock Generator (sheet 1, location D6)

U2 generates a 16.0000 MHz clock as a time base for the 68000 CPU (U1) operation. The clock signal appears on U2 pin 3 as a 16 MHz, 0 to +5 volt square wave.

The binary counter U3 increments the count appearing at its outputs by one for each trailing edge of the clock 16 input. The outputs, therefore, are the 16 MHz input clock divided by 2, 4, 8, and 16. Figure 2-16 shows the binary counter output timing relationships.

2.6.4.2 Reset Control (sheet 1, location C7)

U5, a power monitor control IC, generates a reset signal of at least 200 ms duration at U5 pin 6 each time the +5V supply from the Main Interconnect Power Distribution bus is out of tolerance.

The signal at U5 pin 6 is inverted by the open collector output inverters U6A and U6B; the RESET signal is applied to TP5 and the 68000 CPU RESET and HALT pins 18 and 17 respectively. This signal also connects to the open collector buffers U22A and U22F (2A4). The signal at U22 pin 2 is the VME bus SYSRST signal; the signal appearing at U22 pin 12 is the Serial Bus FPRST signal.

Figure 2-17 shows the reset timing sequence. Note that an undervoltage condition on the +5V supply causes a RESET pulse width of at least 200ms for each occurence of the undervoltage condition.

2.6.4.3 Address Decoding PALS (sheets 1 and 2)

Figure 2-18 shows the interconnection of the VME Microprocessor board Programmable Arrays for Logic (PALs) integrated circuits U10, U13, U14, and U23. U11 and U12 are also shown.

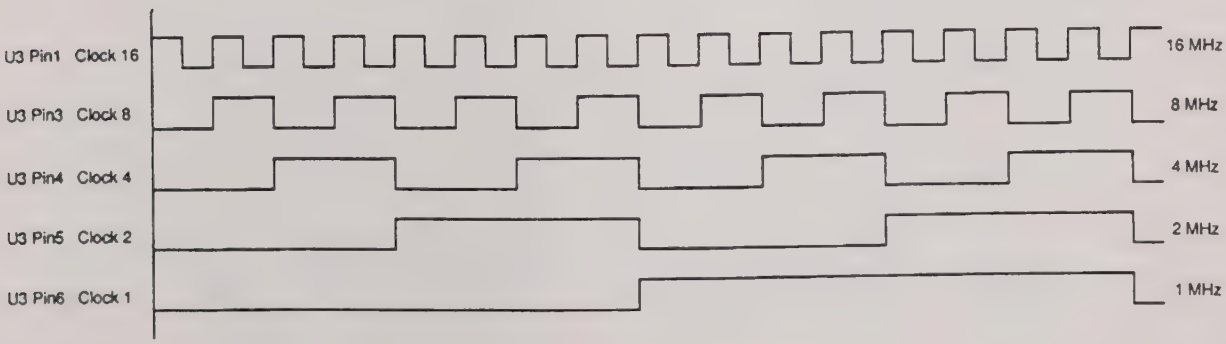


Figure 2-16. System Clock Timing

U10 decodes all on board address spaces on the VME Microprocessor board. Specifically, U10:

1. Decodes the address lines LA15 thru LA20 and the Local Address Strobe (LAS) signal to generate one of the chip selects CSROM0, CSROM1 , CSSRAM0, CSSRAM1, CSDRAM, or one of the peripheral select signals PRPHA PRPHS/.
2. Detects the address of an on-board 8-bit synchronous peripheral on the local address bus and generates the VPA signal as a response.
3. Decodes the AV signal (which indicates the assertion of an interrupt request by an on-board peripheral) to generate the VPA signal required by the VME bus arbitration PAL (U23) during an interrupt acknowledge cycle.
4. Decodes the signal at its own input pin 10 for the generation of the LIACK signal to the VME bus and the VME Bus Arbitration PAL which asserts control of the VME bus during a vectored interrupt acknowledge cycle.
5. Decodes the zero address signal from U9 pin 6 and generates a chip select for the ROM (CSSROM1) containing the reset vector. Only while the 68000 CPU is in a reset condition does the access to location zero occur; in this way the 68000 CPU automatically fetches the reset vector from a location not at location zero (mapped in DRAM), but in ROM.
6. Decodes the OFFBD (Offboard) signal to inhibit the generation of chip selects by U10 when accesses to offboard locations are being made.

Latch U11 controls the selection of the asynchronous peripherals which are the DFI circuit (U55), the System Sync control circuit (U57), and the UARTs U40 and U41.

1. Decodes 0F600H to generate the CSDFI signal (the DFI chip select on pin 9).
2. Decodes 0F500H to generate the CSANL signal (the System Sync chip select on pin 10).
3. Decodes 0F0000H to generate the CSSIO1 signal (the dual UART for front panel communication chip select on pin 15).
4. Decodes 0F1000H to generate the CSSIO2 signal for selecting the test UART 1(U41).

These chip select signals are enabled when both LAS (pin 5) and PRPHA (pin 4) inputs are asserted (logic low).

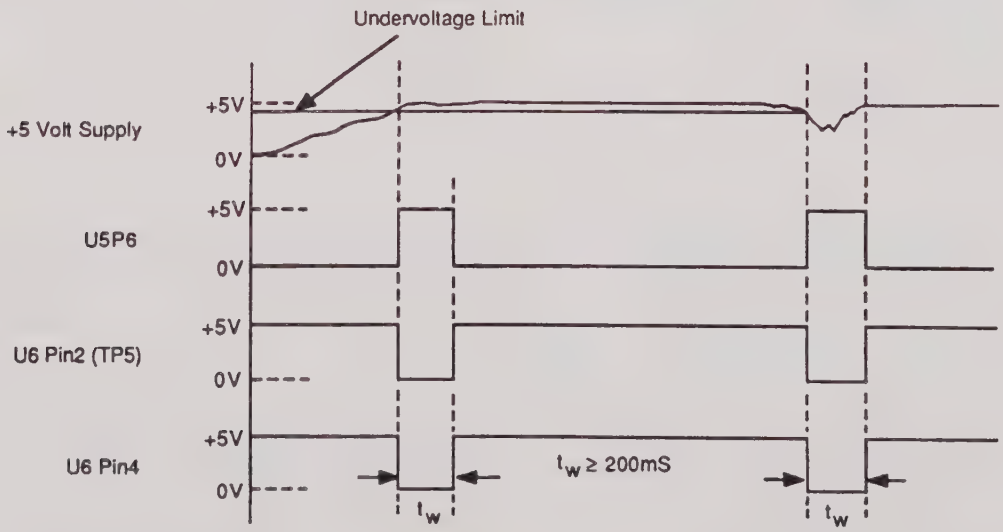


Figure 2-17. System Reset Timing

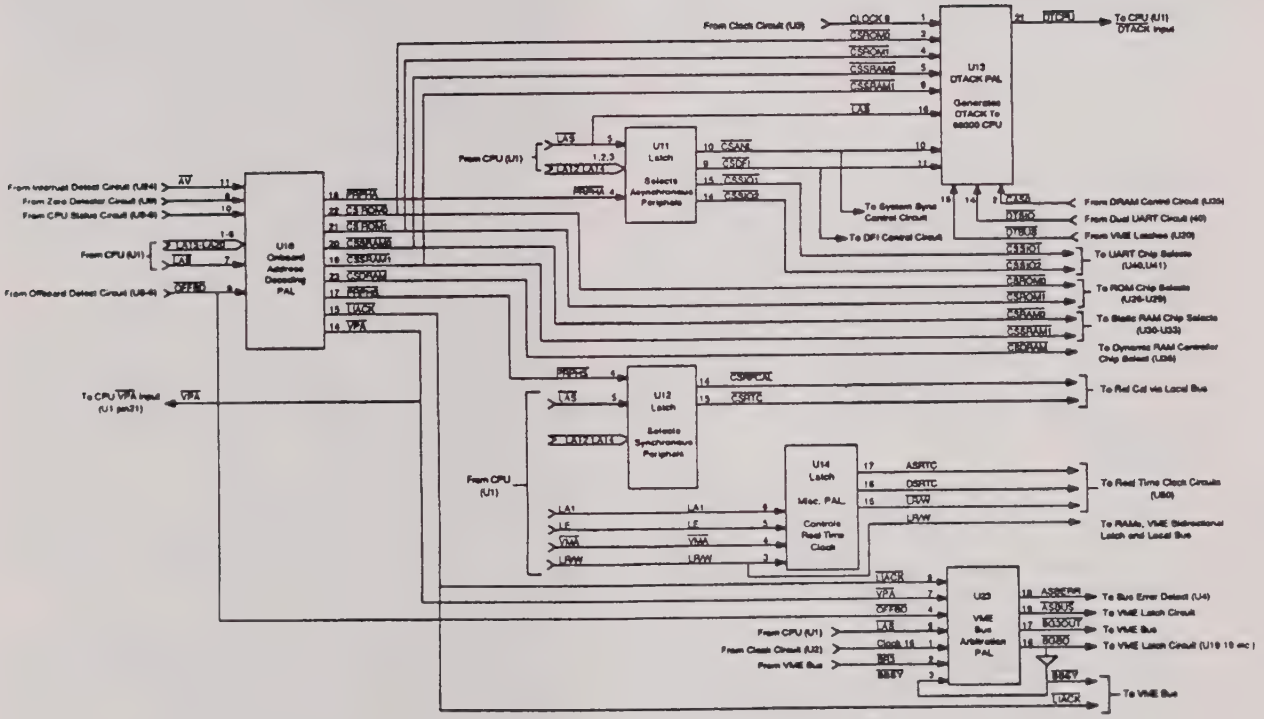


Figure 2-18. PAL Interconnection Diagram

Latch U12 controls the selection of the synchronous peripherals which are the Ref Cal Select (CSRFCAL) and the Real Time clock select (CSRTC). In addition, the miscellaneous PAL (U14) is selected when the CSRTC signal is asserted. See the discussion in paragraph 2.6.4.10 for the timing of the U14 signals associated with the real time clock (U50).

U12 decodes the addresses:

1. 0F90000H to generate the CSRFCAL signal (the Local Bus Ref Cal chip select on pin 14).
2. 0F8000H to generate the CSRTC signal (the real time clock chip select on pin 15).

These chip select signals are enabled when both LAS (pin 5) and PRPHS (pin 4) inputs are asserted (i.e., a logic low).

The 68000 CPU requires the assertion of its DTACK signal (U1 pin 10 and TP2) by an addressed asynchronous 16-bit peripheral when transferring data. The CPU regards the assertion of this signal as a successful data transfer and waits for it before attempting further transfers (more timing information about bus cycles involving DTACK are discussed in paragraph 2.6.4.6 and in the Motorola data sheet for the MC68000).

The DTACK Pal U13 asserts the DTCPU (U13 pin 21, also connected to the 68000 CPU DTACK input P10) signal when:

1. DTBUS is asserted which indicates a successful data transfer over the VME bus (pin 15).
2. DTSIO is asserted which indicates a successful data transfer to the Dynamic RAMs (pin 2).
3. CSDFI is asserted coincident to the CLOCK8 signal (pin 1) indicating that an excessive number of CPU wait states has not occurred during the last data transfer (pin 11).

The DTACK PAL U13 asserts the DTCPU (U13 pin 21, also connected to the 68000 CPU DTACK input P10) signal when the following signals are asserted coincident with the CLOCK8 signal (pin 1).

1. CSANL (pin 10) which indicates a successful write to the System Sync control latch (U57).
2. The ROM and static RAM chip select signals CSROM0, CSROM1, CSSRAM0, CSSRAM1 , coincident with the Local Address Strobe LAS (pins 3, 4, 5, and 9).

2.6.4.4 Interrupt Arbitration (sheet 2, location D2)

All interrupt signals are detected by the priority interrupt encoders U24 and U25. U24 detects the on-board interrupts AV1 through AV6 and the VME bus signal SYSFAIL. U25 detects the off-board interrupts IRQ1 through IRQ7. The binary value of the interrupt priority appears at the encoder outputs A0, A1, and A2 and is recognized by the 68000 CPU (U1) as an interrupt request.

The detection of an on-board interrupt (AV1 through AV6) or SYSFAIL causes U24 pin 15 to go high. When U24 pin 15 goes high, the outputs of U25 are disabled. The off-board interrupts IRQ1 through IRQ7 are not recognized until all of the on-board interrupt signals AV1 through AV6 and SYSFAIL are negated (i.e., a logic high). Because of this, any on-board interrupt has priority over all of the off-board interrupts. The AV signal at U24 pin 14 is asserted whenever an on-board interrupt has been detected; the Address Decoding PAL (U10) uses this signal as its input on U10 pin 11 to distinguish between the type of interrupt (either on-board or off-board) appearing on the interrupt priority lines IPL0 through IPL2.

The 68000 CPU responds to the on-board interrupts AV1 through AV7 with what is called an auto-vectored interrupt acknowledge cycle. The timing diagram for this cycle is shown in Figure 2-19. When one of the auto-vectored interrupts asserts (goes low), U24 encodes the priority and places the binary value of the priority on the signal lines IPL0 through IPL2 (pins 9, 7, and 5 respectively); U24 pin 15 goes high to disable the off-board interrupts and U24 pin 14 (the signal AV) asserts.

The 68000 CPU regards any non-zero value on the IPL lines as an interrupt request and asserts its FC0 through FC2 status outputs (pins 26, 27, and 28) as all ones. U9 pin 8 then goes low. U10 decodes the combination of these signals at the time of the interrupt and generates the VPA signal to the 68000 CPU and to the VME bus arbitration logic. VPA results in the CPU asserting VMA and in asserting the interrupt priority on the Local Address Lines LA1 through LA3 (U1 pins 29, 30 and 31). Therefore, the CPU fetches an interrupt vector from a location in memory defined automatically at the time of interrupt assertion. The auto-vector interrupt acknowledge cycle is complete when the auto-vector is fetched and execution of the interrupt service routine begins.

The off-board interrupt requests IRQ0 through IRQ7 do not cause the generation of the AV signal at U24 pin 14. As a result, the CPU responds with a vectored interrupt acknowledge cycle. During this cycle, U10 responds with the LIACK signal at U10 pin 15. The VME bus arbitration PAL decodes this as a VME bus request and asserts the VME bus signal IACK/. At this time, the off-board interrupt requestor responds by placing on the VME bus lines D0 through D7 data lines the binary value for the interrupt vector and then by asserting DTACK. The CPU then fetches the interrupt service routine vector from a location prescribed in the value provided by the requestor. The vector interrupt acknowledge cycle is complete when execution of the vectored interrupt service routine begins.

2.6.4.5 VME Bus Arbitration (sheet 2, location B2)

The VME bus Arbitration GAL (Generic Array for Logic) U23 decodes its signal inputs to control access to the VME bus; it implements the single level arbitration standard called for in the VME bus Specification Rev C.1 published by Motorola Inc.

U23 pins 16 and 17 change state only with the rising edge of the CLOCK 16 signal at pin 1. The remaining output pins (18 and 19) change independent of the clock signal. The Output Enable, pin 11, is connected permanently to circuit ground; the outputs of the device are always active. The remaining pins (2 through 7) are signal inputs.

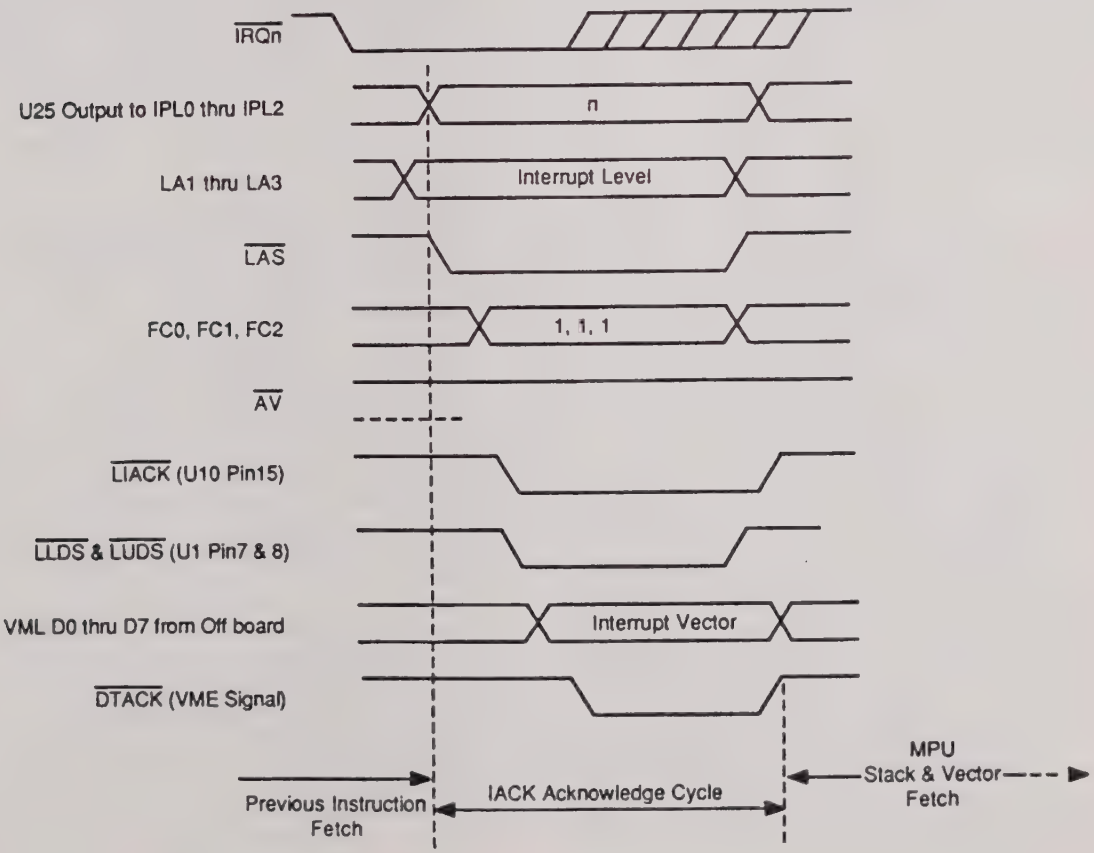


Figure 2-19. Interrupt Response Timing

The VME Microprocessor board only uses the VME-bus when executing instruction at off-board addresses or when servicing off-board interrupts.

Access to the VME-bus initiates with the detection of either an off-board address from U8 pin 6 (OFBD or the assertion of the LIACK signal from U10 pin 15 (see figure 2-20). If the BBSY signal at U23 pin 3 is not already asserted, the BGBD enables all of the VME interface latches U16 through U21. BGBD is also buffered by the open-collector buffer U22C and becomes the VME-bus Bus Busy (BBSY) signal and fed back as an input to U23.

U23 pin 13 asserts coincident with the LAS falling edge and asserts when the ASBUS signal does; pin 13 is programmed as an input/output for the device and has no other connection external to its package.

U23 pin 19 (ASBUS) is the Address Strobe signal for the VME bus and is asserted through U17 pin 17 shortly after BGBD is asserted to assure settling of all data on the VME-bus address and data lines.

Assertion of the U23 input signal VPA indicates a data transfer to a local eight-bit peripheral and hence inhibits assertion of the BGBD signal.

U23 will release BGBD (and thereby BBSY and control of the VME bus) in the event of an auto-vectored interrupt acknowledge cycle or the detection of an on-board address.

Detection of a VME-bus request at U23 pin 2 (BR3) while BGBD is active is ignored until the OFFBD signal goes inactive. Two clock cycles later, U23 asserts the Bus Grant (BG3) output to signal the requesting device that the bus is available. The requesting device then asserts BBSY/. One clock cycle after the requesting device deactivates the request for the bus, it also deactivates the BBSY line; U23 then deactivates the BG3 signal.

The ASBERR signal at pin 18 periodically clears shift register U4; see the description in paragraph 2.6.4.6 for more details.

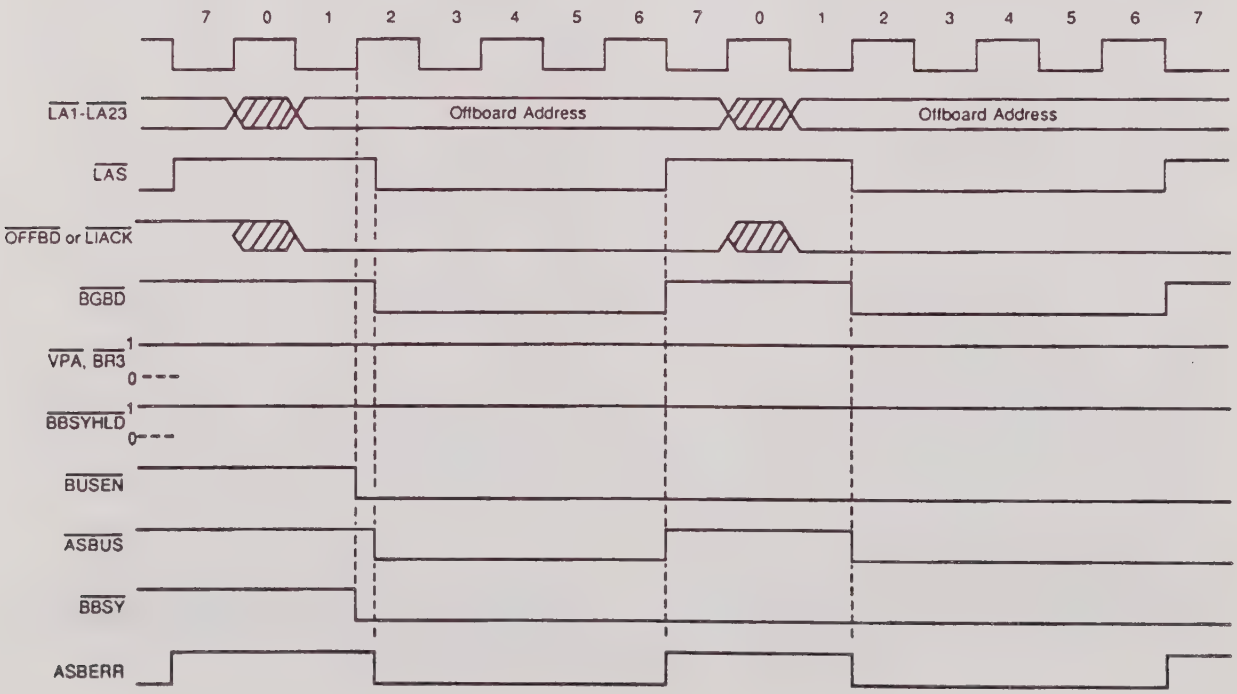


Figure 2-20. VME Bus Arbitration Timing

2.6.4.6 Data Acknowledge (DTACK)/Bus Error (BERR) (sheet 1, location C2)

The 68000 CPU manages asynchronous transfer of data to and from peripheral devices by asserting the necessary bus control signals, waiting for the DTACK response from the addressed peripheral, terminating the control signals, and by waiting for termination of the DTACK signal by the addressed peripheral.

The DTACK PAL (Programmable Array for Logic) monitors all peripheral chip select signals and generates the DTCPU signal from U13 pin 21 to the 68000 CPU pin 10 (DTACK).

The 68000 CPU does not wait indefinitely for the DTACK response. Addressing peripherals that do not exist does not result in the processor waiting forever for a nonexistent peripheral to respond. Instead, only a certain number of clock cycles is allowed to pass while waiting for the response; the 68000 then resorts to exception processing as a result of this bus error so that program execution can continue. In fact, it is this feature that allows the 68000 CPU to identify missing function modules.

A typical data transfer has the following steps:

1. The CPU:
   - Sets the R/W line to the appropriate level.
   - Places the Function Code on FC0-FC2.
   - Places the address on LA1 -LA23.
   - Asserts the Address Strobe.
   - Asserts the upper and lower Data Strobe signals.
2. Next, the addressed peripheral:
   - Decodes the address.
   - Reads or writes data on D0-D15.
   - Asserts Data Transfer Acknowledge (DTACK).
3. The CPU responds with:
   - Latching the data from D0-D15.
   - Negating the Data Strobes.
   - Negating the Address Strobe.
4. The peripheral then negates DTACK/.
5. The CPU then starts the next cycle.

Figure 2-21 shows the timing for a DTACK response.

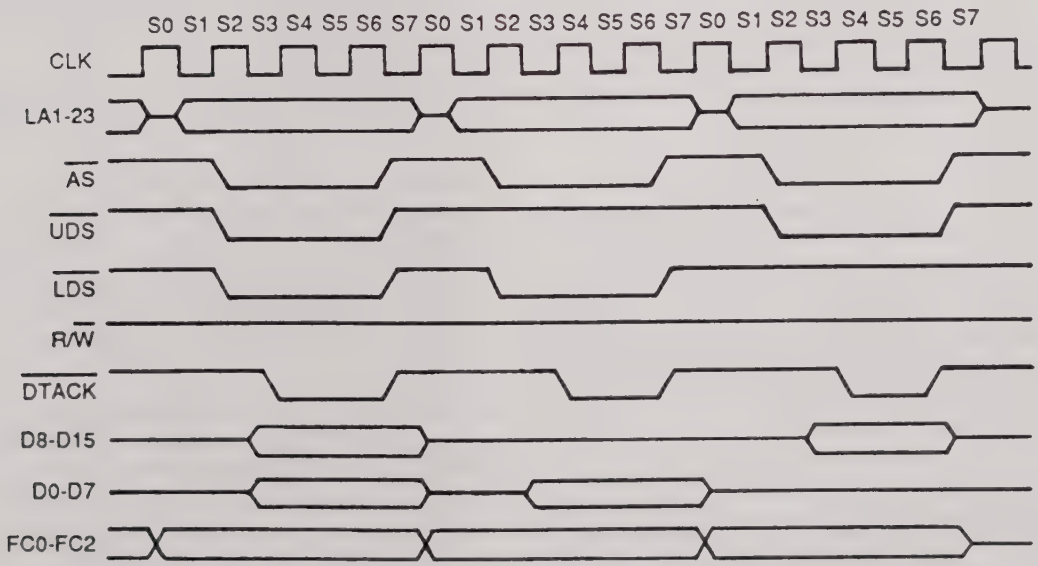


Figure 2-21. DTACK Timing

2.6.4.7 Dynamic RAM (sheet 3, location A3-8)

The Dynamic RAM occupies 256K of address spaces at the addresses 000000H thru 07FFFFH. Memory module U36 is a 512 x 8 dynamic RAM and contains the LD0 through LD7 bits of all dynamic RAM locations. Memory module U37 is also a 512k x 8 dynamic RAM and contains the LD8 through LD15 bits of all dynamic RAM locations.

Dynamic RAMs require that all data locations have their contents periodically refreshed. U35 is an integrated dynamic RAM controller that arbitrates the operation of U36 and U37; it recognizes write and read cycles from the 68000 CPU via the CSDRAM, LR/W, and LAS signals, generates the CASO signal to the DTACK PAL to indicate a successful data transfer, and constantly refreshes in sequence the contents of U36 and U37.

The Local Address bus LA1 through LA18 connect directly to the column and row address inputs 0 through 8 of U35; an internal multiplexer outputs row and column data coincident with the appropriate row and column address strobes (RAS and CAS) to access or write data to the addressed location. Reading or writing from a iven location is controlled by the level of the LR/W ignal.

'he CLOCK8 signal is used as a time base for U35.

'here is no battery backup of the Dynamic RAMs. Loss f the +5V Supply from the Main Interconnect Power)istribution bus results in loss of any data stored in the dynamic RAMs.

2.6.4.8 Non-volatile Static RAM (sheet 3, location B2-3)

U30 through U33 comprise the static RAM circuit and are shown on page 3 of the 68000 VME schematic.

U30 and 31 are 32Kx8 static RAMs and are mapped to locations 1000000H through 10FFFFH. U30 contains the lower byte LD0 through LD7 for these locations and U31 contains the upper byte LD8 through LD15 for these locations. U30 and U31 are selected by the CSSRAM0 signal from the address decoder U10.

U32 and 33 are 32Kx8 static RAMs and are mapped to locations 110000H thru 11FFFFH. U32 contains the lower byte LD0 through LD7 for these locations and U33 contains the upper byte LD8 through LD15 for these locations. U32 and U33 are selected by the CSSRAM1 signal from the address decoder U10.

The upper and lower data strobes LUDS and LLDS are or'd with the LR/W signal to control which upper or lower half of the 16-bit data word appears on the local data bus.

Backup batteries are part of the static RAM integrated circuit packages. Because of this the static RAMs retain data even though the 869 System Power Bus is deenergized. Data retention is guaranteed for eight years from date of battery manufacture.

2.6.4.9 EPROM (sheet 3, location C5-7)

U26 through U29 comprise the EPROM circuit and are shown on page 3 of the 68000 VME schematic.

U26 and 27 are 256K x 8 EPROMs and are mapped to locations 080000H thru 0BFFFFH. U26 contains the lower byte LD0 through LD7 for these locations and U27 contains the upper byte LD8 through LD15 for these locations. U26 and U27 are selected at the chip select input CE on pin 22 by the CSROM0 signal from the address decoder U10.

U28 and 29 are 256K x 8 EPROMs and are mapped to locations 0C0000H thru 0DFFFFH. U28 contains the lower byte LD0 through LD7 for these locations and U29 is selected at the chip select input CE on pin 22 by the CSROM1 signal from the address decoder U10.

The upper and lower data strobes LUDS and LLDS are connected to the 0E inputs of the EPROMs at pin 24 to control which upper or lower half of the 16-bit data word appears on the local data bus.

2.6.4.10 Real-Time Clock (sheet 4, location C1-3)

U6, U49, and U50 comprise the real time clock circuit and is shown on page 4 of the schematic.

Control and data registers within the real time clock chip U50 are accessed via latch U49 which is selected by the CSRTC signal from U12; data direction through U12 is controlled by the LR/W signal from the miscellaneous PAL U14.

U50 generates the on-board interrupt signal AV1 to the Interrupt control circuit U24; the RESET signal from the RESET control circuit on page 1 of schematic brings U50 to its powerup state.

Timing signals required to coordinate transfer of data to and from U50 are ASRTC and DSRTC from the miscellaneous PAL U14 and the LR/W signal.

U50 operates from the backup battery supply (+5VSBY) when the model 869 is turned off and from the Power Distribution Bus +5V supply when the model 869 is turned on. The Real Time Clock always operates regardless of the condition of the model 869 power switch. Diodes CR1 and CR2 isolate the two supplies.

The Real Time Clock time base is the 32.768 kHz crystal oscillator circuit and is independent of any model 869 System Mainframe timing signal.

2.6.4.11 Serial I/O Ports (sheet 4, location B-C7)

The serial I/O ports consist of 2 dual Universal Asynchronous Receiver Transmitters U40 and U41. Operation of the serial I/O ports is selected when the Address Decoder U11 asserts either CSSI01 or CSSI02.

The Port Controller generates a 3.6864 MHz clock which is a baud rate clock for the Terminal, Host, and Monitor ports. This clock should always appear at TP41.

The I/O Processor board clocks the Front Panel Clock (FPCLK) line at 125 kHz; this signal appears at TP40. Data received on the Front Panel Receive (FPRX) line (pin 31 of U40) comes from the I/O Processor board and is synchronized with the Front Panel Clock (FPCLK) line. Serial data is transmitted from the I/O controller to the I/O Processor board via the Front Panel Transmit (FPTX) line (U40 pin 30).

After the RESET signal on pin 34 is asserted, the Serial I/O Port controller ICs U40 and U41 are initialized by the 68000 CPU to the correct operating modes.

The Data Transfer Signal I/O (DTSI0, pin 9) is asserted by U40 to the DTACK PAL to signify a successful data transfer to or from the 68000 CPU.

The Auto-vector interrupt 5 (AV5) is asserted by the I/O controller when the controller has received data from the I/O processor; the 68000 CPU responds to this with an auto-vectored interrupt acknowledge cycle.

The Monitor port interrupt is asserted with AV4; the Terminal and Host port interrupts are asserted on AV5.

U42, and U44 translate their TTL inputs to ±15V output excursions to drive the RS-232 interface connectors P1, P2, and P3; the input levels at U43 and U45 are at the ±15V RS-232 levels and are translated to +5V and 0V logic levels at their outputs.

2.6.4.12 System Sync (SSYNC) Interface

The System Sync control circuit appears on the lower half of page 5 of the 68000 VME schematic.

U57 latches the value of LD0 through LD7 when CSANL is asserted by the decoder U11. The value latched for LD0 at pin 19 determines whether or not the signal appearing at the external Sys Trig In input BNC on the rear panel is transfered to the model 869 SSYNC bus. If U57 pin 19 is a logic low, U58 will not gate the external signal to the SSYNC bus; if it is high, the signal will be gated through.

The U58 outputs are ECL levels (logic '1' = -0.81 V max. and logic '0' = -1.95V min.) The internal SSYNC and the external SYS SYNC IN are wire-or'ed. One will be active and the other deselected.

The selected ECL level sync signal is buffered and level shifted to TTL levels by the two differential pairs Q1 and Q2, Q3 and Q4. An ECL low signal on the SSYNC bus turns Q3 "Off" and Q4 "On". Q4 turns "On" Q1; when Q3 is "Off", Q2 turns "Off". When Q2 is "Off" the voltage appearing at J10 (the rear panel Sys Sync Out BNC) is 0V with a source impedance of 50 ohms set by R61.

An ECL high signal on the SSYNC bus turns Q3 "On" and Q4 "Off". Q4 turns "Off" Q1: when Q3 is "On", Q2 turns "On". When Q2 is "On" the voltage appearing at J10 (the rear panel Sys Sync Out BNC) is near +5V with a source impedance of 50 ohms set by R61.

2.6.4.13 Discrete Fault Indication (DFI) and Relay Driver (sheet 5, location D5)

The DFI relay contacts close when:

1. The model 869 power is off.
2. A 68000 CPU failure occurs.

U55 is a free running counter that will turn off Q5 and K1 if allowed to count to 2^{14}. If K1 turns off, contacts 1 and 4 close. Additionally, U56B inhibits further counts by inhibiting the U55 internal oscillator clock at pin 11. The internal clock frequency is approximately 4 kHz, determined by R57 aqnd C56.

The DFI relay contacts close when the CSDFI signal is not regularly asserted. During the course of normal program execution, the 680000 CPU periodically asserts the address for the CSDFI. When CSDFI or RESET is asserted, the counter U55 is reset to a count of zero, Q5 then remains on, K1 remains energized and the contacts on K1 (pins 1 and 4) remain open.

2.6.4.14 Power Supply Distribution and Bypassing

A table on page 6 of the 68000 VME schematic shows the power supply hookups for each of the integrated circuits on the VME Microprocessor board. The ICs are listed by reference designator.

All power supply bypass capacitors are also grouped on this page by reference designators. Bypass capacitors serve to filter the supply rails at the location of each integrated circuit to eliminate erratic device operation caused by noise.

2.7 THE MAIN INTERCONNECT BOARD (MOTHER BOARD)

2.7.1 Function

The motherboard can be separated into major related signal groups or busses. The function of these busses is to communicate power or information between two points and due to the extreme differences between the busses in relation to signals, speed and line length, each bus required careful design considerations. Some busses have been designed to carry dc power while others conduct frequencies as high as 100 MHz which means that many factors had to be considered including: character line impedance, line termination, module stub length, and driver/receiver requirements.

2.7.2 Block Diagram Description

Figure 2-22 illustrates the block diagram of the model 869 which shows the motherboard's signal groups and their connections.

The 8 layer motherboard not only provides all the necessary interfacing between the mainframe system resources and plug-in modules, but also supports communication paths between the modules themselves. A listing of these internal interfacing busses and their function is given below:

1. External I/O Bus — This bus is connected between the IEEE-488 connector on the back panel and the I/O processor board and provides the communication path between the 869 and the external instrumentation controller.
2. VME Bus — Used by the microprocessor board to input and output command data to the option modules, this bus is basically an extension of the MC68000 microprocessor.

   The VME bus, like many of the other TTL bus terminations utilizes a 3V supply provided on the motherboard, as illustrated in figure 2-23.
3. Local Bus — This bus provides a communication link between the microprocessor board and the Ref/Cal board.
4. System Timing Bus—This bus entails three timing signals, and is simplified in figure 2-24:
   a. A 10 MHz clock for use by logic circuitry throughout the 869.
   b. A system synchronization (SSYNC) line which can provide the necessary timing signals to ensure all modules or instruments are in sync with one another. This signal can be either internally generated or externally supplied.
   c. A system trigger (STRIG) line which initiates certain events to occur when the trigger mode is selected. This signal can be either internally generated or externally supplied.
5. Calibration Bus — Ref/Cal input only bus is used to supply a sampling of voltages and frequencies from each of the plug-in modules for automatic calibration and built-in test (BIT) or self diagnostics.

   Each module slot has its own separate DCV measurement input line to a 3-1/2 digit DVM on the Ref/Cal board, as seen in figure 2-25. In addition, a special DCVCOM line is available for floating or critical measurements where the circuit ground may be too noisy.

   For frequency measurements, each module slot has its own switched line into a frequency counter on the Ref/Cal board as seen in figure 2-26.
6. DAC Bus — This Ref/Cal output bus consists of 16 high resolution analog control lines which drive the modules to control the instruments amplitude, offset or other variable programmed parameters.

   Each module slot has two dedicated 16 bit DAC output lines as seen in figure 2-27.
7. Analog Signal Bus — Not utilized by the model 869.
8. The auxiliary TTL bus provides a communication path between modules for data transfer of digital signals up to 20 MHz.
9. The auxiliary ECL bus will support clock rates of up to 100 MHz and is terminated with a -2V supply.

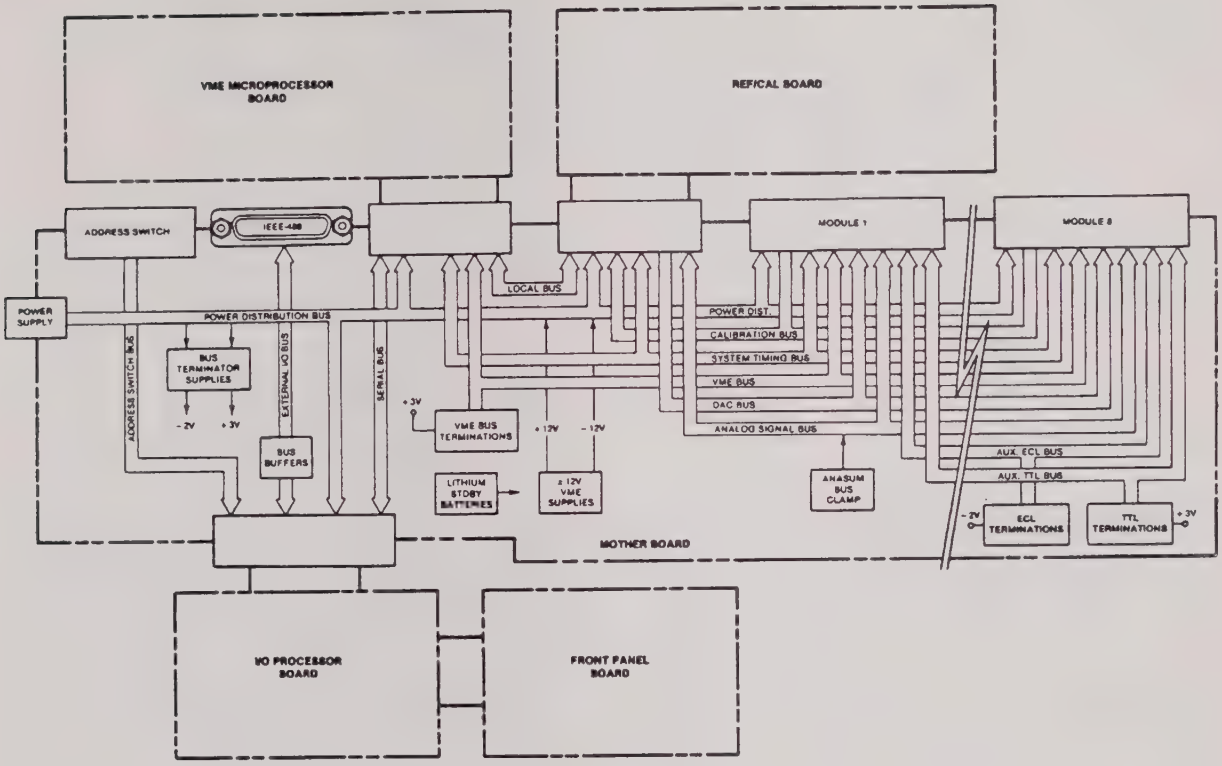


Figure 2-22. Motherboard Block Diagram

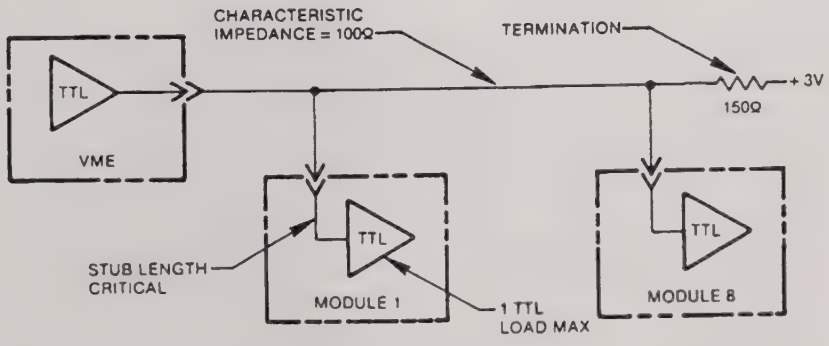


Figure 2-23. Typical VME Bus Signal Line

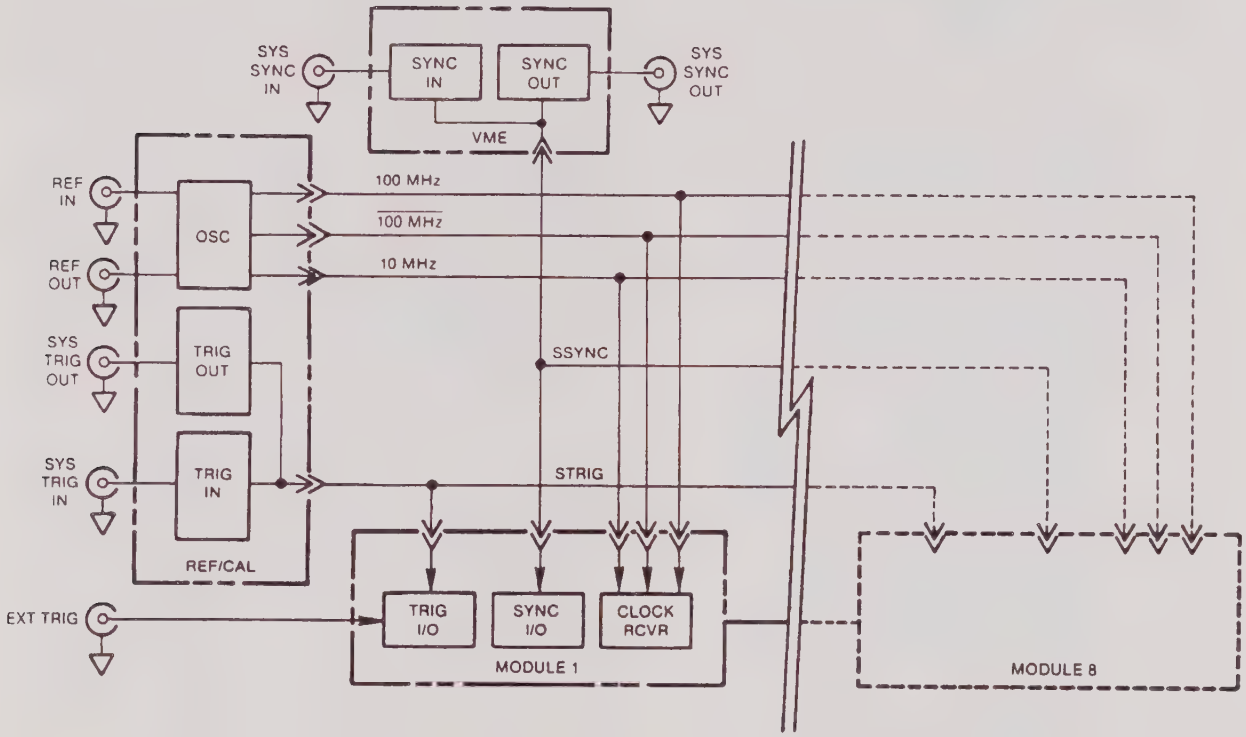


Figure 2-24. System Timing Bus

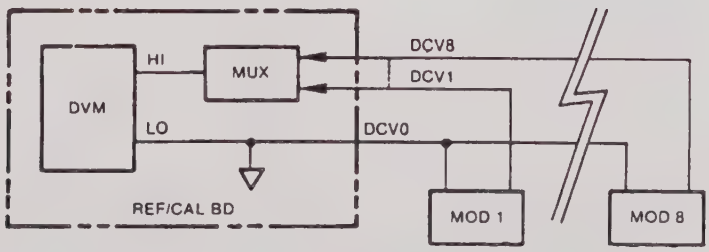


Figure 2-25. Calibration Bus Voltage Measurement Interconnections

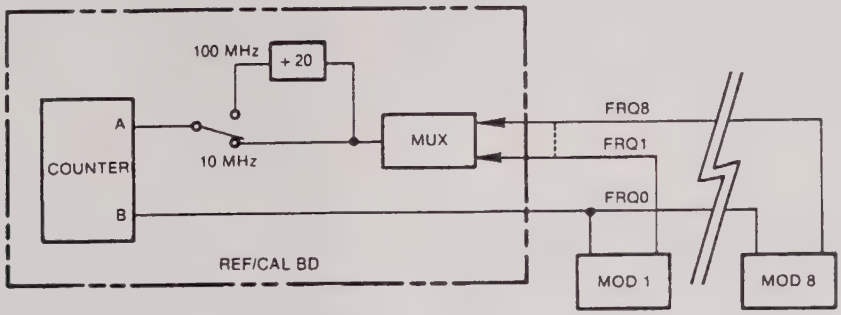


Figure 2-26. Calibration Bus Frequency Measurement Interconnections

10. The power distribution bus connects all the supply voltages originating from the switched mode power supply (+5V, -5V, +15V, -15V, +24V, -24V, +5V isolated and +24V unregulated) and the two reference voltages from the Ref/Cal board (+10V, -10V) throughout the 869 system.

2.7.3 Circuit Diagram Description (Drawing Number 1104-00-3295)

Referring to sheet 1, the sum bus clamp, STRIG/SSYNC, ECL (ECL0-7), clock (10 MHz, 100 MHz), TTL (TTL0-19) and VME resistor terminators are shown. The two lithium batteries, BT1 and BT2 are illustrated at schematic sheet 1, location 5A and are used to provide battery back-up for the real time clock and the static RAM. Sheets 1, 2, 3, and 4 all show the connectors for the 8 modules, the Ref/Cal, VME master board (microprocessor), front panel, power supply and GPIB.

The GPIB buffers U1 and U2, which are mounted on the motherboard and connect to the rear panel GPIB connector, are illustrated in schematic sheet 4, location 6C. Adjacent to the buffers on the schematic is the GPIB address selector which is also mounted on the back panel and connects onto the motherboard.

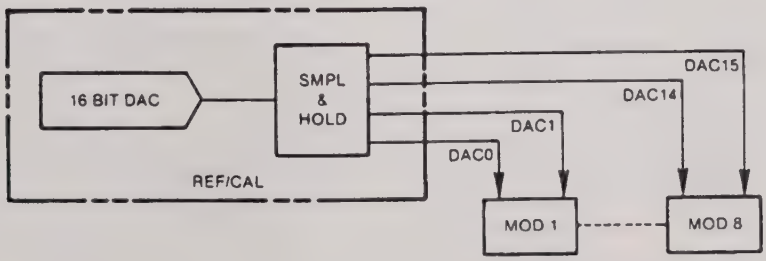


Figure 2-27. DAC Bus

A positive and negative 12V supply are derived from the positive and negative 15V power supply voltages via regulators VR1 and VR2. VR3 and VR4 (schematic sheet 4, location 1,2,A-D) are also voltage regulators used to generate a 3V TTL and 2V ECL termination voltage for the motherboard.

SECTION 3
CALIBRATION

3.1 INTRODUCTION

The Model 869 Multifunction System incorporates a high accuracy, 10 MHz crystal as the reference for all frequency, delay, and period measurements and an internally adjustable reference voltage to which all pulse levels and offsets are calibrated.

There are no internal frequency or level calibration components contained on the mainframe or in the 680-03 Pulse Generator module. The system switching power supply is self regulating and has no voltage level adjustments.

3.2 AUTOCAL AND QUICKCAL

The 869 system pulse generating and timing modules utilize the Autocal method of self calibration. Using this system, output signal amplitude and frequency are measured internally and compensation made, as required, to produce the requested output to the system specification parameters. If the signal is outside of the range of compensation, the Autocal status display will indicate a faulty circuit. The required compensation required for each module output is stored in the non-volatile mainframe memory.

Quickcal provides an Autocal override function for a specific output setup and holds as long as the settings are not changed; if the settings are changed, the parameters revert to the last previous Autocal compensation.

Neither of these calibration operations have any operator or maintenance adjustments, except for the basic reference voltage level, set by adjusting R63 on the Ref/Cal Board.

3.3 CALIBRATION REFERENCE SOURCES

The frequency and level reference sources are located on the mainframe Ref/Cal Board along with the frequency and level measuring circuits. Refer to drawing 1104-00-3385, sheet 4, in Section 5.

The DVM and Gain Select circuit, shown at the top of sheet 4, illustrates the circuitry for the digital voltmeter used for level calibration. The selected level is input to IC U36, a 12-bit binary (plus sign and overrange) dual slope integrating A/D converter. This unit has the high accuracy and low drift required to make measurements in the ranges defined by the 869 specifications. The loss through the signal path is of a minimal value and does not affect the level of accuracy required by the system specifications.

The resolution of the A/D converter is one part in 4096 or 224 ppm, therefore the stability of the reference voltage is the major factor in the overall absolute accuracy of the circuit. The +2 Volt Reference used is developed from the +10 VR level, as shown on the schematic, sheet 4, lower right corner. The +10 VR level is developed from the +15 volt bus from the mainframe switching power supply. This triple level of regulation provides an optimum +2 volt reference for the circuit.

Because of component aging and other considerations, the 2 volt reference is adjustable. This adjustment is the only actual calibration adjustment in the system, including the modules previously defined as using Autocal and/or Quickcal.

The Frequency Counter and Select circuit, shown in the center of sheet 4, illustrates the circuitry for the digital counter used for frequency calibration. The selected frequency is input to IC U20, a Wavetek developed programmable universal counter/timer which uses a Plessy CLA3000 Series LSI device as a basis. The selected input is applied at U33 pin 39. The divide by 20 device, U31, is not used in the present system configuration. The FREQ0 input is also not used.

Counter U33 uses the 10MCLK line as a reference; this is the direct output of U14, a temperature controlled crystal oscillator, operating at 10.0000 MHz. The maximum error of this frequency source will not affect the level of accuracy required by the 869 specifications. The crystal oscillator circuit is shown on sheet 2 of the schematic diagram.

Cumulative circuit delays developed between the module output monitor and counter U33 do not affect counter accuracy, since they are much smaller that the deviations allowed by the specified parameters.

3.4 +2 VREF VOLTAGE ADJUSTMENT

Trimpot R63 , the 2 volt reference adjust, can be accessed from the top edge of the Ref/Cal module without removing the module or using extender boards. Test points TP1 (ground) and TP3 (+2VREF) are next to R63 and are also accessable. Refer to drawing 1101-00-3385 for component location.

Test equipment required includes a calibrated voltage source (Datel DVC-8500-A, or equivalent), a DVM with at least 5-1/2 digit resolution (Datron 1065, or equivalent), and a low loss cable from the voltage source with a BNC connector on one end.

Proceed as follows:

1. Connect voltage reference and DVM to the Cal In connector on the rear of the Ref/Cal board. Set reference voltage to +4.000V ±200 μV, as read on external DVM.
2. At 869 mainframe front panel, perform setup as follows:

   Press Channel Select and keypad 0 keys
   Press F4 DIAG key
   Press F2 REF/CAL key
   Press F2 DVM key
   Press F3 MODE key
   Press F1 SINGLE key
   Press F2 RANGE key
   Press F1 X1 key
   Press F1 CHANNEL key
   Press keypad key 9 and EXECUTE

3. Press F6 READ key; if required, adjust trimpot R63 for a readout of +4.000 volts on the mainframe front panel display. Press the F6 READ key for each reading update.
4. Connect DVM to TP1 (gnd) and TP3; voltage indicated should be approximately +2.049 volts.
5. Change voltage source in 1 volt increments, pressing F6 READ key for each change, through -4.000 volts. Verify correct readings on mainframe front panel display.

3.5 10 MHz REFERENCE ADJUSTMENT

The 10 MHz frequency reference source is located on the mainframe Ref/Cal Board. Refer to drawing 1104-00-3385, sheet 2.

The 10 MHz reference adjustment screw can be accessed by removing the paper hole cover from the 10 MHz crystal (U14) located at the top rear of the Ref/Cal Board. Refer to drawing 1101-00-3385 for the component location.

The test equipment required is a HP model 5334A frequency counter or equivalent, a 50 ohm in-line termination, and a three foot, 50 ohm BNC male/male coaxial cable.

Proceed as follows:

1. Remove power to the model 869 mainframe. Place the Ref/Cal Board on the module extenders and apply power. Leave the front panel control in their power-up condition.
2. Connect the frequency counter input to the Ref/Cal connector "Ref Out" (J101) on the rear of the Ref/Cal board using a 50 ohm coaxial cable. Place the 50 ohm termination at the frequency counter input.
3. Adjust U14 for a readout of 10,000,000, ±5 Hz or less on the frequency counter display. A small non-metallic screwdriver or alignment tool should be used.

SECTION 4
TROUBLESHOOTING

4.1 INTRODUCTION

This section provides fault isolation information to help troubleshoot the 869's mainframe resources. There is also additional data to help determine if the problem is in the mainframe or in a module. Refer to the 680-03 Maintenance Manual for troubleshooting the Pulse Generator module.

This section is organized to provide troubleshooting information to fault isolate a specific complaint provided by the operator or to provide a set of procedures to identify and fault isolate an unknown problem.

The operator's identified problem will generally come from the Mainframe Verification Procedure, Table 2-4 of the 869 Operator's Manual, or from a System (mainframe) Selftest or AutoCal error code. Table 4-1 below provides a fault isolation paragraph for each symptom listed.

Table 4-1. Initial Fault Isolation.

Mainframe Resource Fault	Test Paragraph
Power Up Test	4.2
Selftest Error	4.2.1
AutoCal Error	4.2.2
Beeper Test	4.5.6
Display View Angle Test	4.5.7
Back Light Test	4.5.8
10 MHz Reference Test	4.6.2
System Trigger Test	4.6.4 / 4.6.5
Temperature Sensor Test	4.6.6
Time Display Test	4.7.12
System Sync Test	4.7.13

Alternately, you may choose to follow the troubleshooting procedures in sequence and systematically identify the nature of the fault.

There is an Initial Operational Check to power-up the model 869 and test its functions for normal operation. If you do not obtain the indicated results from the Operational Check, then proceed on with the equipment tests.

The equipment tests should isolate the problem to a specific area, and then by reviewing the correct operation of the suspected faulty circuit in the theory of operation (Section 2 of this manual), the circuit can be tested in more detail.

4.1.1 Test Equipment Requirements

Table 4-2 lists the common and specialized test equipment and fixtures required to complete all of the tests and procedures described in this section:

Table 4-2. Required Equipment/Fixtures

Equipment	Description
Oscilloscope	Tek 465 or Equiv.
Digital Multimeter	Fluke 8840A or Equiv.
Frequency Counter	HP 5334A or Equiv.
Signal Generator	Wavetek 278 or Equiv.
Extension Card (2 ea.)	Wvtk P/N 1100-00-3212
Extension Card (1 ea.)	Wvtk P/N 1100-00-1615
Extender Cable Assy.	Special IDC male/female Contact Wvtk for info.

4.2 OPERATIONAL CHECKS

In this section, you will check the normal power-up operation of the model 869 to determine which functions do not operate properly. This should help you to quickly isolate the problem. Refer to Section 2 of Operators Manual for returning the equipment for factory repair.

If you do not obtain the indicated results, then go to the appropriate paragraph as indicated in Table 4-1 and 4-3. Try to resolve each problem as you encounter it, and then do this operation check again to verify correct power up message.

Connect the model 869 to an ac receptacle and then press the rear power switch on. Press the "On/Stand-by" front panel switch to "On" and observe the power-up message, which should resemble one of the following four displays:

1. Correct Power-Up Display Message:

   WAVETEK Model 869
   Ver x.x.x

   Indicates: Front Panel, VME microp and Ref/Cal board (partially) are operatio eed on with the Selftest and AutoCal te her isolate any problem(s) which may y(the mainframe or in any of the Pulse Ge od- ules.

4. Incorrect Power-up display message:

   WAVETEK Model 869

   Indicates: Problem in front panel "E witch located on rear panel or associated w

2. Power-Up Display Error Message:

   Front Panel
   Ver x.x

   Indicates: Ref/Cal board is not plugge rectly or is malfunctioning. If problem still exer it is reinstalled, proceed to Ref/Cal equipme para- graph 4.6.

3. No display message, but power is pres green front panel LED is ON:

   Indicates: VME microprocessor, Ref/Cal o pro- cessor, front panel display, or the I/O bo is not plugged in or is malfunctioning. If problem exists after boards are reinstalled, proceed to p graph 4.4 for fault isolation.

4. No display message and no power present – ren front panel LED is off:

   Indicates: Power supply problem. Proceed to par graph 4.3, Power Supply Tests.

4.2.1 Isolation with 869 Selftest Facility

The Global Selftest will help fault isolate between the mainframe and the Pulse Generator modules. To perform the Global Selftest, program the following key sequence: **Channel Select**, **9** (all), **Cal/Test**, selftest (**F2**) and start (**F1**).

The Global Selftest will consume approximately 25 seconds for the mainframe (system) and 2 minutes per Pulse Generator channel module installed. If no Selftest errors are detected, the display will appear as follows when Selftest is complete:

```
Global self test status: 000h   all

------self test------
START  abort  status
```

If any Selftest error is detected, the "000h" display will be replaced with a Global Selftest error code. The global error code is the bit-weighted sum of all mainframe/ modules with an error. The error code identifies the location of the error, whether in the mainframe system or in which channel, not the type of error. Running the Selftest again with Channel Select set to the number of the identified module will identify the failed parameter.

Since the least significant bit of the bit-weighted error code is the mainframe, any odd valued error code includes the mainframe. A mainframe error code should be cleared before troubleshooting a channel module error code, because system resources within the mainframe are used to Selftest the failed module parameter. An even, non-zero Selftest code indicates a failure in one of the channel modules, which should be handled in the 680-03 Maintenance Manual.

For an odd-valued Selftest error, perform a system Selftest by programming the following keys: **Channel Select**, **0**, **Cal/Test**, selftest (**F2**), and start (**F1**). The parameter which caused the previous Global Selftest error should fail again and be identified. The error code returned from the system self test is the sum of the individual error codes for each signal tested, and will either be zero if all tests have passed or a hexadecimal number representing the failed test(s).

Error Code	Test1	Test2	Test3	Test4	Test5
Pass	0	0	0	0	0
Fail	1	2	4	8	16

For example, an error code of "3" would indicate that tests 1 and 2 had failed.

The Model 869 System Selftest is composed of five subtests. Four of these tests check signal paths and components using an onboard counter. One test uses the onboard DVM.

Test 1

Signal tested	Tol	Error	Description
10 MHz clock	0.005%	1	System reference clock

This test measures the frequency of the 10 MHz system reference clock (U14). It tests the external reference signal only if it is selected. Since this same signal is used as the frequency reference for the counter being used to test it, we do this test only to verify the signal path and operation of the counter circuitry.

Test 2

Signal tested	Tol	Error	Description
10 MHz oscillator	7%	2	Synchronous oscillator, gateable

This test measures the frequency of the 10 MHz synchronous gateable oscillator circuit (U17) using the onboard counter to a tolerance of 7%.

Test 3

Signal tested	Tol	Error	Description
175 kHz oscillator	5%	4	DVM integration oscillator

This test measures the frequency of the 175 kHz DVM oscillator circuit (U36) using the onboard counter to a tolerance of 5%.

Test 4

Signal tested	Tol	Error	Description
Internal trigger	0.1%	8	System trigger reference

This test measures several frequencies derived from the 10 MHz clock by the internal trigger circuitry (U17, 26, 27) using the onboard counter to a tolerance of 0.1%. The frequencies 5, 10, 50, 100, 500 Hz and 1 kHz are measured by the onboard counter using period average mode.

The frequencies 5, 10, 50, 100, 500 kHz, 1 and 10 MHz are measured by the onboard counter using gated mode with a gate time of 100 ms.

Test 5

Signal tested	Tol	Error	Description
Temp	15-35°C	16	System Temperature reference

The DVM is set up to monitor the temperature near the rear of the Ref/Cal Board by measuring the voltage from the LM35DZ temperature sensor (CR9). A measurement in the range of 15 to 35 degrees Celsius (depending on room temperature) gives a rough indication that the DVM chip is working.

All circuit blocks tested by mainframe Selftest are on the Ref/Cal Board. Refer to Table 4-3 for troubleshooting paragraph numbers for each observed Selftest error.

4.2.2 Isolation with 869 AutoCal Facility

The Global AutoCal will further fault isolate between the mainframe and the Pulse Generator modules. To perform the Global AutoCal, program the following key sequence: **Channel Select 9** (all), **Cal/Test**, AutoCal (**F1**) and start (**F1**).

The Global AutoCal will consume no noticeable time for the mainframe (system), but it requires 4 minutes per Pulse Generator channel module installed. If no AutoCal errors are detected, the display will appear as follows when AutoCal is complete:

```
Global calibration status: 000h   all

----automatic calibration-----
START abort enable disabl status
```

If an AutoCal error is detected, the "000h" display will be replaced with a Global AutoCal error code. The discussion in the previous paragraph pertaining to Selftest error codes applies identically to AutoCal error codes.

An even, non-zero AutoCal code indicates a failure of a parameter to calibrate in one of the channel modules, which should be handled in the 680-03 Maintenance Manual.

For an odd-valued AutoCal error, first perform a System Selftest (System Selftest checks more Ref/Cal items than a System AutoCal) by programming the following keys: **Channel Select**, **0**, **Cal/Test**, selftest (**F2**), and start (**F1**).

Identify the failed test from the error code and refer to Table 4-3 for troubleshooting paragraph numbers for each observed Selftest error.

If the returned unit passes Global Selftest and Global AutoCal and the reason for return is still unknown, perform the Mainframe Verification, Module Verification, and Performance Verification procedures to locate the fault or out of tolerance condition before returning the unit to the user.

Table 4-3. Troubleshooting Error Codes

Failed Test	Troubleshooting Paragraph
Test 1	Para 4.6.2
Test 2	Para 4.6.5
Test 3	Para 4.6.2
Test 4	Para 4.6.5
Test 5	Para 4.6.6

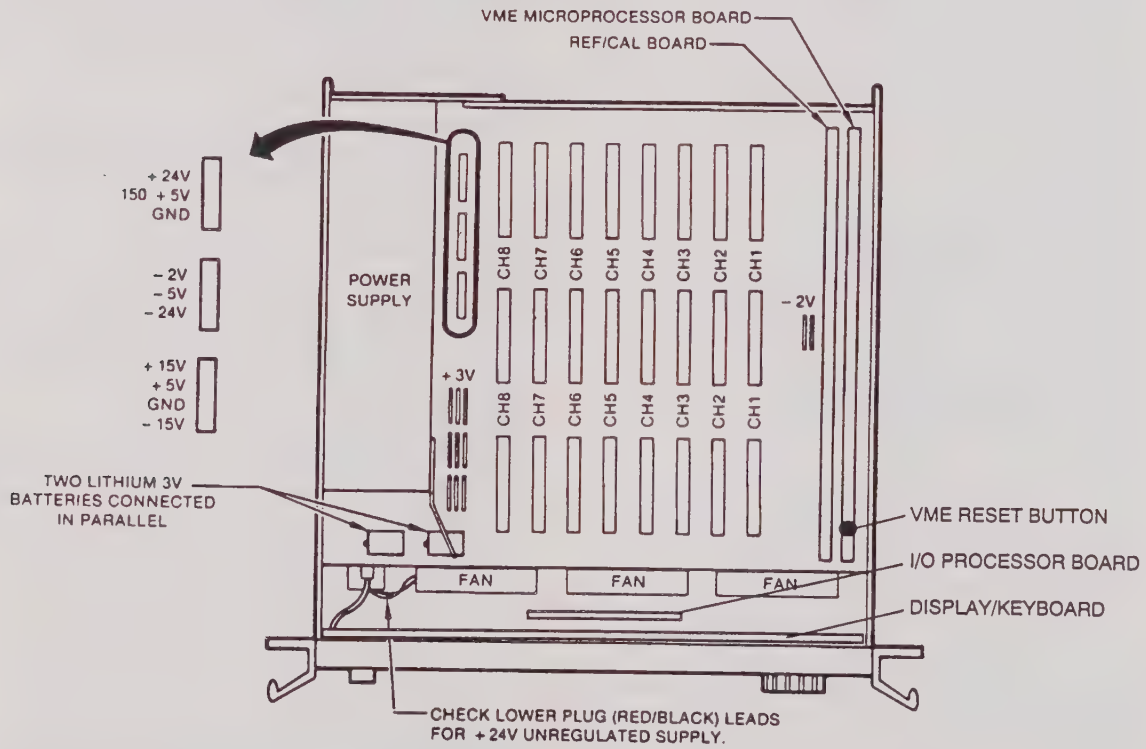


Figure 4-1. Power Supplies and Board Locator

Table 4-4. Power Supply Voltage Distribution

PS Voltages	Isolated +5V	+5V	+15V -15V	+24V -24V	+24V Unregulated	-2V -5V
Boards or devices Powered	Front panel and I/O board	all boards and modules	Ref/Cal Bd, VME Board, and 680-03 Channel Module	680-03 Channel Module (Output Ampl)	Fans only	680-03 Channel Module (ECL)

4.3 POWER SUPPLY TESTS

If no turn-on display message appears and there are no indications of power (green front panel LED off — fans off) being present, proceed with the following checks:

1. Verify power source and inspect power cord, plug and connector.
2. Check the fuse on the rear panel.
3. If the problem still exits, check the ac input to the power supply. If ac input is OK, locate, referring to figure 4-1, the dc test points on the mother board and then verify the power supply dc outputs shown in table 4-1.
4. Once a faulty power supply voltage is located, use standard connector/module removal and replacement technique to isolate the problem to either the power supply or a module/board. The power supply is a single replaceable assembly (Wavetek P/N 1204-00-2943).

4.4 FAULT ISOLATION - NO POWER-UP DISPLAY

This section provides some preliminary troubleshooting data to quickly isolate the cause of a blank panel display after turn-on. The 869 mainframe has three microprocessor circuits on three different assemblies. A complete or "fatal" failure of any one of these microprocessor systems, as well as a failure of the Display/Keyboard itself, can cause the display to be blank. The troubleshooting procedures in this section will attempt to fault isolate a blank indication to a single assembly, and then provide the paragraph number of a detailed troubleshooting procedure for the suspected assembly. The serial communication link between the VME Processor and the I/O Processor, and then the Local Bus between the VME Processor and the Ref/Cal Processor, will be used as a quick means of microprocessor system fault isolation. If the communication link between two microprocessor systems is active, then both have to be operating (at least at the internal bus structure level).

1. Power on the unit and verify no display message, but the green power LED is on.
2. Verify normal Local Bus communication activity between the VME Processor Board and Ref/Cal Board microprocessors as follows:
    a. With power off, remove the Ref/Cal Board (refer to Figure 4-1 for board locations) and install two 96-pin extender cards (Wavetek P/N 1100-00-3212). Reinstall the Ref/Cal Board on the extender cards and power up the unit.
    b. Check pins J2A31/A32 with oscilloscope for a 10 MHz reference signal (a squarewave of approximately 1 Vp-p amplitude).
    c. Check pins J2A29/A30 with oscilloscope for 10 MHz inverted reference signal (a squarewave of approximately 1 Vp-p amplitude).
    d. Check pin J2A18 with oscilloscope for the LR/W signal (a pair of negative pulses repeated every 15.5 μs, approx. 5 Vp-p).
    e. Check pin J2B18 with an oscilloscope for the CSRC/ signal (a dc level of approximately +5 Vdc).
    f. Check pin J2A7 with oscilloscope for the LE signal (a positive 0.5 microsecond pulse of approximately 5 Vp-p amplitude).
    g. Check the following Local Bus connector data lines with oscilloscope for normal bus activity: J2A13 thru A16 and J2B13 thru B16.
    h. Check the following Local Bus connector address lines with oscilloscope for normal bus activity: J2A8 thru A11 and J2B7 thru B11.
3. Verify normal Serial Bus communication activity between the VME Processor Board and I/O Processor Board as follows:
    a. With power off, remove the I/O Processor Board (refer to Figure 4-1 for board locations) and disconnect the 34-pin ribbon cable from J1. Install the narrow 64-pin extender card (Wavetek P/N 1100-00-1615) on J30 of the motherboard. Install the 34-pin extender ribbon cable assembly on J1 of the I/O Processor Board. Reinstall the I/O Processor Board on the extender card, connect the ribbon extender cable (observe the correct polarity), and power up unit.
    b. Check pin J2A1 with oscilloscope for the FPRST/ (SYSRST/) signal (a static dc level of approximately +5 Vdc, 0 Vdc when VME Processor Board "Reset" switch is pressed).
    c. Check pin J2B1 with oscilloscope for the FPCLK signal (a 125 kHz TTL squarewave).

NOTE

For the following checks, observe the static waveform and then press a front panel key. The waveform should briefly change frequency and return to the static frequency.

d. Check pin J2A2 with oscilloscope for the FPTX signal (a group of 4 negative pulses, one 16 μs pulse and three 8 μs pulses, repeated every 12 ms). Press any front panel key and observe momentary change in frequency.

e. Check pin J2B2 with oscilloscope for the FPRX signal (a group of 4 negative pulses, one 16 μs pulse and three 8 μs pulses, repeated every 12 ms). Press any front panel key and observe momentary change in frequency.

If the checks in Step #2 indicate missing or incorrect signal(s) but Step #3 checks were correct, troubleshoot the Ref/Cal Board microprocessor circuits. Refer to paragraph 4.6 and schematics 1104-00-3385.

If the checks in Step #3 indicate missing or incorrect signal(s) but Step #2 checks were correct, troubleshoot the I/O Processor Board microprocessor circuits. Refer to paragraph 4.5 and schematics 1104-00-3236.

If both Step #2 and Step #3 indicated missing or incorrect signal(s), troubleshoot the VME Processor Board microprocessor circuits. Refer to paragraph 4.7 and schematics 1104-00-3409.

4.5 DISPLAY AND I/O BOARD TESTING

If no display message is present and no power is evident (green LED on the front panel is off), then check the isolated 5V input with isolated ground to the I/O Processor and front panel Keyboard/Display boards.

NOTE

Power to the I/O Processor board and to the Display/Keyboard is isolated (ISO+5, ISOGND) except for one side of the isolated serial interface (U10, 11 optical isolators). TP1 is non-isolated GND and TP2 is ISOGND connection for connecting test probes.

If power is present (green front panel LED is on) but no message is displayed, troubleshoot the I/O processor and then Display/Keyboard per the following paragraphs:

4.5.1 Troubleshooting a Fatal Failure

1. Verify that the front panel enable switch on the rear panel is on (refer to Sect. 2. Operators Manual).
2. Check that SYSRST from VME Processor Board resets the 6803 microprocessor on the I/O Processor Board:

   a. With power off, lift the I/O Processor Board (refer to Figure 4-1 for board locations) enough to remove P1 ribbon cable in upper right corner of the board, and then remove the I/O Processor Board entirely.

      Install the 64-pin narrow extender card (Wavetek P/N 1100-00-1615) and replace the I/O Processor Board on the extender. Extend the ribbon cable with the ribbon cable extender and reconnect it to the I/O Processor Board. Power up the unit.

   b. Connect oscilloscope probe from TP2 (common) to the right-hand side of R10 (by U11 in lower right of I/O Processor Board).

      Observe a TTL high. Press and then release the RESET BUTTON on the top front of the VME board (right-most board in the chassis). The 6803's MR/ signal should go low and then return high during a VME SYSRST.

   c. If reset signal is not as defined above, first verify the SYSRST signal at U11 pin 3 (TP1 common), and then troubleshoot the U11 circuit.

3. Check 8 MHz clock at model 6803 microprocessor (U1-40, pins 2 and 3).
4. Verify mode 2 initialization of 6803 during reset:

   a. Press and hold the VME reset button.

   b. Connect oscilloscope probe from TP2 (common) to U1 pins 8 (low), 9 (high) and 10 (low, approximately +1V).

   c. Release the reset button. If any of the signals were not as described above, troubleshoot the associated U1 circuitry.

5. Verify 6803 interrupt lines, pins 4 and 5, are high.

NOTE

In the following steps, the MC6803 microprocessor system signal lines will be observed with an oscilloscope probe. If two adjacent pins are momentarily shorted together with the probe tip, it is extremely likely that the microprocessor will discontinue processing the ROM instructions and data in a normal fashion. When this occurs the signals will change characteristics from what is described (generally appear more periodic and at a lower repetition rate). This can be easily corrected by momentarily pressing the VME reset button.

6. Check the following model 6803 microprocessor signal outputs for activity (refer to figure 2-7):
   a. E CLK, pin 40 – 2 MHz (0.5 μs) TTL square.
   b. AS, pin 39 – 2 MHz period, 25% duty cycle.
   c. Address Bus lines, pins 22-29 – Activity on all lines; TTL lows and highs evident. Check for "stuck" lines.
   d. Address/Data bus lines, pins 30-37 – Activity on all lines; TTL low, high and tri-state levels evident. Also verify demultiplexed Address lines at U2, pins 12-19.
   e. R/W, pin 38 – TTL high with 0.5 μs low pulses occurring at irregular intervals.
   f. Troubleshoot any "stuck" lines by isolating devices.
7. Verify Address Decoder PAL (U4) outputs the following chip/port select signals:
   a. ROM2/, pin 22 – Enables the ROM (U6); continuously active signal with TTL low and high states evident. Also verify U6, pin 22 has E/ square wave signal.
   b. RAM CS/, pin 20 – Enables the RAM (U5); continuously active signal with TTL low and high states evident.
   c. KEYBD/, pin 19 – Scans the keyboard rows. A short burst of low pulses at a 20 ms rate (very low duty cycle; use normal triggering and high beam intensity on oscilloscope).
   d. DISPLAY/, pin 18 – Enables the display Address Decoder. A burst of low pulses (a few ms) which occurs at each key press. Use normal triggering and high oscilloscope beam intensity to detect.
   e. GPIB/, pin 17 – Selects the GPIB port (U3). Continuous low duty cycle pulses, much higher repetition rate than front panel signals.
   f. WE/, pin 15 – Controls read/write operations in the RAM (U5); continuously active signal with TTL low and high states evident.
   g. Verify E/ signal [same as a) under step 6] at ROM, U6 pin 22.
   h. Troubleshoot any "stuck" lines by isolating devices.
8. Verify the serial interface to the VME processor is operating:
   a. Verify E clock signal at U10, pin 6 (TP1 common).
   b. Verify signal activity at U10, pin 7 (TP1 common). If serial interface is operational, 6803 transmit signal should be a short burst of low pulses at an approximate 1 ms rate.
   c. Verify signal similar to b) above, the VME processor's transmit signal, at U11, pin 7 (TP2 common).
   d. If one of the above is missing, both are missing. The fault can be due to either the I/O Processor or the VME Processor. Troubleshoot by verifying that other I/O Processor signals are correct, and that the inputs and outputs of U10 and U11 match each other, even if incorrect. Then go to the VME Processor troubleshooting paragraph and verify key signals.
9. If none of the above signal lines is "stuck", but the processor does not seem to be processing ROM instructions and data properly, a device may be defective. Check/replace PROCESSOR (U1), EPROM (U6), RAM (U5) and/or address decoder (U4).
10. If the Processor system is operating correctly as described above and the front panel display is still blank, continue with the test paragraphs in this section.

NOTE

The following paragraphs (4.5.2 to 4.6) provide troubleshooting data to aid in fault isolation when power supplies are on (green LED on front panel is on), but the display is blank or nonsensical. These tests assume that the I/O Processor tests of the preceding paragraph were performed and uncovered no problems with the Address/Data bus, the A0 through A3 Address lines, the R/W line, or the DISPLAY/ line. Circuits and test points referred to can be located with schematic 0103-00-3124 and parts locator 1100-00-3124.

WARNING

Removal of the Front Panel Assembly exposes the operator to dangerous voltages. The front panel standby power switch operates on logic levels, and is not dangerous, but the LCD backlight power supply (T1) outputs 500 Vp-p, 700 Hz which appears on connector J3.

4.5.2 Display Tests

Perform this test if paragraph 4.5.1 indicated that I/O Processor signals are normal, and the front panel display is inoperative.

1. Remove the front panel assembly as follows:
   a. Place the I/O Processor Board back in its connector slot without the extender card, but leave the ribbon cable extension on.
   b. Remove the power cord.
   c. Invert the unit and remove the bottom cover by removing the two screws and tilting the cover up from the rear until the lip is disengaged at the front panel.
   d. Return the unit to an upright position, and verify that the mother board is not making contact with any conductive object which may short out motherboard traces.
   e. Remove one screw and one retainer extrusion at the front end of each side panel-mounted handle strap. Retain the spacer under each.
   f. Remove two screws from the front of each side panel extrusion (not from the handle extrusion).
   g. Pull the panel forward and lay it down on the surface in front of the unit.
   h. Plug in the power cord and turn the unit on.
2. Identify connector J3. Do not come in to contact with the high voltage present on this connector.
3. Ground reference the scope probe to TP2.
4. Verify A1, A2, and A3 signals at U1 pins 1 through 3. Use "normal" scope triggering, negative slope, and high beam intensity to verify the DISPLAY/, E1, E2 and register strobe signals at U1 pins 4 15, 14 and 13.
5. Check the emitter of Q2 for a voltage in the approximate range of -1 to -2 Vdc.
6. Check ribbon cable, J1, and the LCD display device, DSP1. The ribbon cable can be removed at DSP1 and probed for correct signal activity. If no signals are missing, the display should be replaced.

4.5.3 Keyboard Tests

Perform this test if paragraph 4.5.1 indicated that I/O Processor signals are normal, and the front panel keyboard is inoperative.

1. If not already done, perform steps 1 through 3 of paragraph 4.5.2.
2. Verify the Address lines at the inputs of U7 and U8, and the Address/Data lines at the output of U6. Verify the KEYBOARD/ signal at U6 pin 1 per step 7c of paragraph 4.5.1.
3. Column output pins of U7 and U8 are normally low, unless a key in the selected column is held down. Row inputs to U6 are normally high unless a key in the selected row is held down. When a key is held down, its column and row lines have an Address signal on them. Column 1, U7 pin 1, is under the **F1** key. Vertical columns across the panel, left to right, correspond to column lines at the outputs of U7 and U8, left to right across the schematic. Likewise, Row 1 is at the top of the panel (**7**, **8**, and **9** keys) and Row 5 is at the bottom.
4. With the information in the previous step, check each key and its corresponding Column and Row signal to isolate the problem to U6, U7, U8, or to a keyboard section, KB1 to KB4.

4.5.4 Control Knob Tests

Perform this test if paragraph 4.5.1 indicated that I/O Processor signals are normal, and the front panel control knob is inoperative.

1. If not already done, perform step 1 of paragraph 4.5.2.
2. Ground reference the oscilloscope probe to TP2 (Iso-gnd) of the I/O Processor Board.
3. Verify TTL level signals, ø1 and ø2, are generated at U12 (I/O Processor Board) pins 8 and 12 as the control knob is rotated. If missing, troubleshoot control knob and interconnections.
4. If ø1 and ø2 signals are present, but knob is not operative, troubleshoot U12 and U13 circuit on I/O Processor Board.

4.5.5 External I/O (GPIB) Test

Set the address switch to address 9, and then use an instrument controller interfaced with the model 869 over the External I/O bus to send the following command:

10 *IDN (identify yourself)

The model 869 should, if the address switch and all associated circuitry are operational, respond with the following message:

Wavetek Model 869
Ver X.X.X

If no response message is obtained, check address switch on motherboard and at input to I/O Processor Board. Also check U3 (GPIA) and associated circuitry.

4.5.6 Beeper Test

Pushing each key on the keyboard should result in a beep. If no beep is present verify the power-up display message is on the model 869 display.

Press the CHANNEL SELECT and 0 keys to select the mainframe, and then the Utility (**F1**), Frtpnl (**F1**), and Beep (**F1**) keys. The "Beep" menu selections are "on" (**F1**) and "off" (**F2**). Current selection will be in upper case letters. If beep does not operate after "ON" is selected, check U14 and associated circuitry on the I/O Processor Board.

4.5.7 Display Viewing Angle Tests

The viewing angle of the display can be adjusted between 0 and 45°.

To change viewing angle, press the following keys.

CHANNEL SELECT 0
Utility (**F1**)
Frtpnl (**F1**)
View (**F2**)

Now enter a numeric value or parameter by all three methods to check the controls:

- 0-9 keys
- Four arrow cursor
- Control knob

At 0°, the display contrast will appear highest when looking at the display straight on. If the viewing angle does not change, check U4, Q2 and associated circuitry on front panel Display/Keyboard.

4.5.8 Backlight Test

Press the CHANNEL SELECT and 0 keys to select the mainframe, and then the Utility (**F1**), Frtpnl (**F1**), and Lite (**F3**) keys. The "backlight" menu selections are "on" (**F1**) and "off" (**F2**). Current selection will be in upper case letters.

If light does not operate after "ON" is selected, check the display 3-pin connector, U4, Q1 and oscillator on the front panel Display/Keyboard.

4.6 REF/CAL BOARD TESTS

Troubleshooting of the Ref/Cal Board will generally be initiated by 1) turn-on message indicating a "fatal" failure of the Ref/Cal microprocessor, 2) Selftest error code from Table 4-3, or 3) a systematic completion of troubleshooting tests.

A microprocessor failure may be indicated by the turn-on message, "Front panel, Ver X.X", per paragraph 4.2, step 2

This can occur because the VME Processor Board is up and running and can communicate with the front panel/IO Processor Board; however, the VME Processor Board cannot communicate with the Ref/Cal Board. Verify the +5V, -5V, +15V and -15V supplies to this board and carry out the following tests.

4.6.1 Troubleshooting a Fatal Failure

1. Identify the Ref/Cal Board using Figure 4-1 and, with power off, remove the board from the chassis. Install two extender cards (Wavetek P/N 1100-00-3212) and replace the Ref/Cal Board on the extender cards. Power-up the chassis.

   Check the +5V supply on the Ref/Cal Board (for instance at FB3). If +5V is not present, check the supply distribution on the board.

   Refer to the power supply hookup chart on the schematic to find all ICs connected to +5V.

2. Check the 6803 clock signal at U5 pin 2, with the oscilloscope. There should be a 4 MHz signal. If not, check/replace the microprocessor chip U5, crystal Y1, or caps C6, C7.

   Verify 1 MHz "E" clock at U5 pin 40, and 1 MHz 25% duty cycle pulse (AS) at U5 pin 39. If signals are not present, verify CR1 and CR17 diodes and pull-up resistors R2 and R3 (10Ω).

3. Turn the model 869 off. Check the reset pulse at test point TP2 with the oscilloscope. When turning the model 869 back on, the signal at TP2 should be low for approximately 200 ms and must stay high afterwards. If not, check SYSRST continuity.
4. Check/replace EPROM U1, address latch U2 and/or data latch U3.
5. Check/replace RAM U7 and/or transceiver U10.
6. Check/replace address decoders U4, U9, U8 and/or U58.
7. Check that SYSRST from VME Processor Board resets the 6803 microprocessor on the I/O Processor Board:
    a. Identify the I/O Processor Board using Figure 4-1 and, with power off, remove the board from the chassis. Install a narrow extender card (Wavetek P/N 1100-00-1615) and replace the I/O Processor Board on the extender card. Power-up the model 869.
    b. Connect oscilloscope probe from TP2 (Iso-gnd) to the right-hand side of R10 (by U11 in lower right of I/O Processor Board).

       Observe a TTL high. Press and then release the RESET BUTTON on the top front of the VME Processor Board (right-most board in the chassis). The 6803's MR/ signal should go low and then return high during a VME SYSRST.
    c. If reset signal is not as defined above, first verify the SYSRST signal at U11 pin 3 (TP1 common), and then troubleshoot the U11 circuit.
8. On the I/O Processor Board, check the 8 MHz clock frequency at the 6803 microprocessor (U1-40, pins 2 and 3).
9. On the I/O Processor Board, verify mode 2 initialization of the 6803 microprocessor during reset:
    a. Press and hold the VME Board reset button.
    b. Connect oscilloscope probe from TP2 (Iso-gnd) to U1 pins 8 (low), 9 (high) and 10 (low, approximately +1V).
    c. Release the reset button. If any of the signals were not as described above, troubleshoot the associated U1 circuitry.
10. On the I/O Processor Board, verify that the 6803 interrupt lines, pins 4 and 5, are high.

NOTE

In the following steps, signal lines in the MC6803 microprocessor system will be observed with an oscilloscope probe. If two adjacent pins are momentarily shorted together with the probe tip, it is likely that the processor will discontinue processing ROM instructions and data in a normal fashion. When this occurs the signals will change characteristics from what is described (generally appear more periodic and at a lower repetition rate). This can be easily corrected by momentarily pressing the VME reset button.

11. On the I/O Processor Board, check the following model 6803 microprocessor signal outputs for activity (refer to figure 2-7):
    a. E CLK, pin 40 – 2 MHz (0.5 μs) TTL square.
    b. AS, pin 39 – 2 MHz period, 25% duty cycle.
    c. Address Bus lines, pins 22-29 – Activity on all lines; TTL lows and highs evident. Check for "stuck" lines.
    d. Address/Data bus lines, pins 30-37 – Activity on all lines; TTL low, high and tri-state levels evident. Also verify demultiplexed Address lines at U2, pins 12-19.
    e. R/W, pin 38 – TTL high with 0.5 μs low pulses occurring at irregular intervals.
    f. Troubleshoot "stuck" lines by isolating devices.
12. On the I/O Processor Board, verify that the Address Decoder PAL (U4) outputs the following chip/port select signals:
    a. ROM2/, pin 22 – Enables the ROM (U6); continuously active signal with TTL low and high states evident. Also verify U6, pin 22 has E/ square wave signal.
    b. RAM CS/, pin 20 – Enables the RAM (U5); continuously active signal with TTL low and high states evident.
    c. KEYBD/, pin 19 – Scans the keyboard rows. A short burst of low pulses at a 20 ms rate (very low duty cycle; use normal triggering and high beam intensity on oscilloscope).
    d. DISPLAY/, pin 18 – Enables display Address Decoder. A burst of low pulses (a few ms) which occurs at each key press. Use normal triggering and high oscilloscope beam intensity to detect.

e. GPIB/, pin 17 – Selects the GPIB port (U3). Continuous low duty cycle pulses, much higher repetition rate than front panel signals.

f. WE/, pin 15 – Controls read/write operations in the RAM (U5); continuously active signal with TTL low and high states evident.

g. Verify E/ signal [same as step 6a] at ROM, U6 pin 22.

h. Troubleshoot any "stuck" lines by isolating devices.

13. On the I/O Processor Board, verify that the serial interface to the VME processor is operating:

a. Verify "E" clock signal from U10 pin 3 at U10 pin 6 (FPCLK).

b. Verify signal (FPRX) activity at U10, pin 7 (TP1 common). If serial interface is operational, 6803 transmit signal should be a short burst of negative pulses at an approximate 1.2 ms rate.

c. Verify the VME Processor's transmit signal (RCVR), signal similar to b) above, at U11-7 (TP2 Iso-gnd).

d. If one of the above is missing, both are missing. The fault can be due to either the I/O Processor or the VME Processor.

Troubleshoot by verifying that the other I/O Processor signals are correct, and that the inputs and outputs of both U10 and U11 match each other, even if incorrect. Then go to the VME Processor troubleshooting paragraph and verify key signals.

14. On the I/O Processor Board, if none of the above signal lines are "stuck", but the microprocessor does not seem to be processing the ROM instructions and data properly, a device may be defective.

Check and/or replace PROCESSOR (U1), EPROM (U6), RAM (U5) and/or address decoder (U4).

NOTE

Do not continue with any of the following paragraphs unless the Ref/Cal Board powers up with no front panel error.

4.6.2 Internal Oscillator Tests

1. Press Channel Select, 0, Utility, Diag, Ref/Cal, and Test. This internal self-test will verify proper operation of the counter, 10 MHz reference, 10 MHz oscillator, DVM oscillator, and internal trigger frequencies of 10, 100, 1k, 10k, 100k, 1M, and 10 MHz.
2. Verify +10.00V reference at R49 and -10.00V reference at R52 (9.995 to 10.005 Vdc). Refer to schematic 1104-00-3385, sheet 4.
3. Verify 10 MHz reference output at J101 BNC by connecting to oscilloscope: 5 Vp-p unloaded, 2.5 Vp-p into 50Ω. Verify rise/fall time <10 ns into 50Ω load.
4. Connect to frequency counter and verify 10 MHz ±1 ppm (9.99999 MHz to 10.00001 MHz).
5. Connect Wavetek Model 278 sync output to UUT Ref in BNC (J100).
6. Set model 278 to 10.10 MHz.
7. Select model 869 to SYSTEM (Internal Reference).
8. Verify counter reading of 10.1 MHz. If no signal is present, check operation of TCXO (U14), comparator (U15), Mux (U16), and Q1, Q2, Q3.
9. Verify the 175 kHz DVM oscillator frequency. Connect frequency counter to U36 pin 22. Verify frequency of 175 kHz +/-5%. Refer to schematic 1104-00-3385, sheet 4.

4.6.3 Voltage Reference Tests

1. Connect +4.000V ±200 μV from voltage reference source to the external CAL INPUT BNC J104 on the Ref/Cal board.
2. Press Channel Select, 0, Utility, Diag, Ref/Cal, Dvm, Mode, Single, Range, X1, Channel, 9, Exec, and Read.
3. Adjust pot R63 for a readout of +4.000V on the model 869 front panel display (approx. 2.049 Vdc @TP3). Continue to select the READ key to update the dvm reading.
4. Change calibrator input to +3V, +2V, +1V, 0V, -1V, -2V, -3V and -4V and verify display readouts.
5. To verify troubleshoot the 2.048V reference: Measure the voltage at TP3. It should be around +2.048V. If not, check/replace U50, U29, Q4, RN2, or R63.

4.6.4 Internal Trigger Circuit Tests

1. Reset the model 869 to its power-on state.
2. Press Channel Select, 0, Config, Config, and Internal.
3. Set Frequency to 10,000, and press Execute.
4. Connect trigger output BNC J103 to the oscilloscope and verify a 10 kHz square wave. Level should be +2.4V into >10Ω and >1.2V into 50Ω. Rise/fall times should be >5ns.

   If no signal is present, check the PLL loop U21, U22, U24, and U25 and/or trigger select MUX U23 and latches U12 and U13.
5. Change the trigger frequency from 10 kHz to 1 MHz and verify on the oscilloscope.

4.6.5 System Trigger Circuit Tests

1. Press Channel Select, 0, Config, Config, Off and then verify on oscilloscope the 0V level at J103.
2. Press Manual Trigger and verify on oscilloscope the positive-going pulse.
3. Press External, Normal, Level, 1.5, Exec, and Pos.
4. Set the Wavetek 278 to 50 kHz, and connect the sync output to the model 869 Ext Trig Input (J102). Verify 50 kHz trig out (J103) on the scope. If signal is not present, check comparator U17, DAC U26, or amplifier U27. Refer to schematic 1104-00-3385, sheet 2.
5. Press Level, 8, Exec and verify trigger out at +5V level.
6. Press Level, 2, Exec, and verify trigger out of 50 kHz.
7. Press Level, -8, Exec, and verify trigger out at +5V level.
8. Press Level, 2, Exec, and verify trigger out of 50 kHz.
9. Connect model 278 to both model 869 trig in and to oscilloscope Ch1 with a tee connector.
10. Connect model 869 trig out BNC J103 to oscilloscope Ch2. If signal is not present, check U17, U54, U18 and U19.
11. Select Slope, Pos, Neg, Pos, and verify 180° phase shift on the oscilloscope.
12. Select System, Trigger, External, Events, 4, Exec, and verify 12.5 kHz on the oscilloscope (50 kHz/4).
13. Select 10, Exec, and verify a 5 kHz square wave (50 kHz/10).
14. Select System, Trigger, External, Delay, 5^{-6}, Exec. Verify a 5 μs delay time between model 278 output and model 869 Trig Out pulse on oscilloscope CH1 & CH2.

4.6.6 Temperature Sensor Test

Press Channel Select, 0, Util, Temp, On and then verify that the temperature sensor is operating by displaying the present temperature (~30°C) on the left hand side of the second display line.

1. If the display indication is missing or greatly different than expected, check CR9, U52, and U35. Refer to schematic 1104-00-3385, sheet 4.

4.6.7 Amplitude/Offset Control Circuit Tests

1. Press Channel Select, 0, Utility, Diag, Ref/Cal, Shdac, Channel, 0, Exec, Level, 3, and Exec. Monitor this voltage with a DVM on the backplane J24 pin C31.

   Using the cursor keys, decrease the amplitude in steps of 1V until an amplitude of -3V is reached. Verify the amplitude changes on the DVM.
2. Repeat Step 1 for channels 1-15. Select the shdac channel, then increment the voltage and monitor the DVM. Channel 1 is on J24 pin A3, channel 2 is on J21 pin C31, channel 15 is on J3 pin A31.
3. If either of step 1 or 2 amplitude changes were successful, measure the +15V and the -15V supply voltages. If these voltages are not present, check the board's supply distribution.

   Also check the -10V supply. If all of the supplies are OK, check/replace registers U37, U38, U39, U40, address decoder U4 and D/A converter U41.
4. If some of the step 1 and 2 checks were successful, but not all of them, check/replace the components responsible for the failed amplitude/offset sample & hold function. U42 through U49, Q6 through 21, C96 through Cl27 and RN5 through 8.

   Also check/replace select register U39, U40 (each sample & hold is updated every 8 ms. These pulses can be verified with the oscilloscope at the outputs of U39, U40).

4.7 VME PROCESSOR BOARD TEST

If no display message is present on the display after the VME Processor and IO Processor Boards are reinstalled, proceed on with this test to determine why the VME Processor Board has not initialized itself and the other boards in the model 869 system mainframe.

4.7.1 Pre-power-up Check Out

The following simple tests should be carried out initially so that fundamental problems like short circuits between the supplies and ground do not cause an incorrect diagnosis later on in the test sequence.

Short circuit
An ohm meter should be used to test for power supply shorts to ground. Clip the ground lead of the ohmmeter to TP10 or TP20 (GND) on the VME Processor Board.

1. Test for isolation of TP20 (+5V) from GND
2. Test for isolation of P28-C32 (+15V) from GND
3. Test for isolation of P28-C1 (-15V) from GND
4. Test for isolation of P28-C3 (-5V) from GND
5. Test for isolation of P28-A28 (-2V) from GND

4.7.2 Test Configuration

1. Configure the Model 869 chassis with Ref/Cal Board and the I/O Processor Board.
2. Insert the extender cards in the VME Processor Board slot making sure that the VME bus connector has a 96-pin extension. Check for bent or broken connector pins. Check that the connector is properly seated.
4. Install the VME Processor Board on the extender cards.
5. Turn the model 869 power switch from Standby to "On".

4.7.3 Power-On Test

Depending on what happens here, there are several courses of action to take.

1. If front panel displays ""Model 869" message press the System "SYSTEM" key and verify that the System menu is displayed. If the System menu is operational, proceed to the SELF TEST section. If the System menu cannot be displayed proceed to paragraph 4.7.11 (Front Panel Communication).
2. If front panel display remains the same connect probe from oscilloscope to TP1 (LAS) and look for a low active signal with an amplitude of +5 volts and a frequency of about 1 MHz. Press and release the RESET button on the top of the board and observe the LAS signal.
   a. LAS signal is present and remains active. Unit is hung up or communication to the front panel is obstructed. Proceed to paragraph 4.7.11 (Front Panel Communication).
   b. LAS signal is present for a moment and then stops. Unit has a problem with DRAM or faulty ROM. Proceed to paragraph 4.7.10 (DRAM Tests).
   c. LAS signal just goes high from tri-state. Serious CPU (U1) or bus problem. Proceed to paragraph 4.7.5 (68000 CPU Bus Test).
   d. LAS signal goes low. Problem with bus error circuit (U4). Proceed to paragraph 4.7.8 (BUS ERROR Circuit Tests).

4.7.4 Power Supply

Several points on the board should be tested for the presence of the required power supplies.

4.7.5 68000 CPU Bus Test.

Using the DVM, the 68000 address, data and control bus should be tested for shorts to supply or ground and also between any two adjcient lines. If a short is indicated, remove the 68000 microprocessor and retest. If the short is disappears, replace the 68000 microprocessor chip. If the short remains, test all peripheral chips connected to the shorted lines.

4.7.6 CLOCK Circuit Test.

a. Check for 8 Mhz CPU clock on TP3. Make sure this same signal appears on U1-15. If a 8 Mhz signal is not present check for a 16 Mhz signal from U2-3.

b. If a 16 MHz signal is present check pins and supplies on U3 and replace if these are OK.

c. If a 16 Mhz signal is not present, check supply pins on U2 and check that U2-8 is not grounded. If supplies are OK and signal is not grounded, replace U2.

4.7.7 RESET Circuit Tests

a. Check for a static high at TP5 (RESET) and U1-17. Verify TP5 and U1-17 momentarily goes low when the RESET button on the top front of the VME Processor Board is pressed.

b. If a low signal is not there, check for high signal on U5-6 when S1 (RESET) is pressed. Replace reset button if the signal is not present.

4.7.8 BUS ERROR Circuit Tests

a. If TP1 (LAS) remains low and TP4 (BERR) is not also low then the bus error circuit is faulty.

b. Check for presence of 2 MHz clock on U4-8.

c. Check for U4-1, -2, and -9 all high. If this signal is low, then problem lies in the BUS ARBITRATION PAL (U23).

d. Check 16 MHz clock to U23-1. Fix open circuit if not active.

e. Check for U23-5 (LAS) low. Fix open circuit if this is not low.

f. Check for U23-3 (BBSY) high. Fix short to ground if this is low.

g. Replace BUS ARBITRATION PAL (U23)

4.7.9 ROM Tests

NOTE

Before testing the ROM chips ensure that the chips are installed in their sockets correctly, that is, as far to the right (toward the 68000 microprocessor U1) as possible. The alignment key will be on the left.

CAUTION

If it is determined that the ROM chip(s) has been installed incorrectly and power has been applied to the model 869, then it is almost certain that the chip(s) in question have been damaged. If this is the case, troubleshooting the ROM circuits would be a waste of time as the chip(s) must be replaced.

NOTE

When reading the chip pin numbers it should be noted that the ROM chip pin numbers and the schematic ROM socket pin numbers will not be the same for the 64K ROM chips, but will be correct for the 128K chips. During troubleshooting using the schematic, subtract 2 from the pin number shown on the ROM socket to find the correct pin on the ROM chip.

a. ROM0 (ROM ZERO)

(1) Chip select signals. Check for the presence of the CSROM0 signal on U28-22 and U29-22. Check for the presence of the LLDS signal on U28-24 and the LUDS signal on U29-24.

(2) Verify all Address and Data lines on U28 and U29 for normal bus activity.

(3) If any bus line is not active and shows a continuous low level, check line for short.

(4) Replace ROMS U28 , U29.

b. ROM1 (ROM ONE)

(1) Chip select signals. Check for the presence of the CSROM1 signal on U26-22 and U27-22. Check for the presence of the LLDS signal on U26-24 and the LUDS signal on U27-24.

(2) Verify all Address and Data lines on U26 and U27 for normal bus activity.

(3) If any bus line is not active and shows a continuous low level, check line for short.

(4) Replace ROMS U26 , U27.

4.7.10 DRAM Tests

A DVM and oscilloscope can be used to perform the following checks to determine if any bus lines are shorted together. This test also tests continuity of the address and data lines to the DRAM and SRAM.

a. RAS refresh strobe. Check that the RAS strobe at TP35 has a low active pulse with a period of about 15 μs. Make sure this strobe is reaching the DRAM SIMMs at U36-27 and U37-27.

b. CAS strobe. Check that the CASU and CASL strobes appear on U36-2 and U37-2. These are low active strobes with period of about 1 second.

c. Address Line continuity to the DRAM controller. Check address lines LA1 through LA18 for continuity from the 68000 CPU (U1) to the DRAM controller (U35). A discontinuity in an address line makes it appear that data is written to the wrong address.

d. Check all Multiplexed Address Lines for continuity.

e. Check all Data Bus Lines for continuity.

4.7.11 Front Panel Communication Tests

The VME Processor Board communicates to the I/O Processor Board through a 68681 DUART (U40). During a normal power up sequence the VME processor sends the "Model 869" message and then periodically sends a 0xAA character to the I/O Processor.

The I/O Processor should respond by sending a 0xAA character back to the VME processor. If this communication link is broken there is no way to control the Model 869.

The DUART output to the front panel could be fed back to the input at the P2 connector. A X1 clock input could be derived from SYSCLOCK on the P1 connector.

Software in the ROM writes an 0xAA to the front panel periodically. The frequency at which the 0xAA is written determines whether the 68000 received a response. This would test the continuity of the FPXMIT, FPRCV and FPCLK lines to P2. Refer to schematic 1104-00-3409, sheet 4.

a. FPCLOCK. Check for the presence of a 125 kHz clock signal on TP40 (FPCLOCK). Check that the signal appears on U40-2 and U40-39.

b. FPTX. Check for a low active pulse from U40-30. During normal operation this signal will be a group of 4 negative pulses (one 16 μs pulse and three 8 μs pulses) repeated every 12 ms.

   If this signal is missing, check for the CSSI01/ signal at U40-35. This should be a low active signal with a width of 0.8 μs. There should be a long series (approximately 0.5 ms wide) of these pulses followed by a pause. Trace these signals back to the 68000 CPU through U11 and U10. Absence of CSSI01/ indicates the CPU is hung up elsewhere, possibly with the RTC.

c. FPRX. If the FPTX signal is present, check for the presence of the FPRX signal on U40-31. This signal should be identical in shape and period to FPTX. If this signal is missing check for continuity of FPRX to P28-A3 and FPTX to P28-A4.

4.7.12 Real Time Clock Tests

The MC146818 real time clock chip (U50) is at a base address of 0xF8000. It is a synchronous peripheral with a multiplexed address and data bus. This is handled by separately writing the address and the data while maintaining the chip select low. During normal operation this chip generates an interrupt at 32 Hz rate. The chip is read once to clear this interrupt. Once every second the time is read from the chip. Refer to schematic 1104-00-3904, sheet 4.

a. Oscillator. Check that the 32.768 kHz oscillator is functioning at TP50. If missing, check power to U50 and for bad component values in R50, R51, C51, C52, and C53. Check CR1 and CR2. As a last resort replace the crystal (Y50). They sometimes break when dropped.

b. Chip select. Check for the presence of the low active signal CSRTC on U12-15, U14-2 and U49-19.

c. 32 Hz interrupt. Check for the presence of the 32 Hz interrupt while the unit is running. This should appear as a low active strobe with a frequency of 32 Hz on U50-19 and U24-11.

4.7.13 System Sync Tests

The following tests require that only one 680-03 module be installed in the mainframe. Turn the model 869 off and place the VME Processor Board on two extender cards (Wavetek 1104-00-3212). Apply power to the model 869.

1. Verify an output at J10 when the internal 680-03 pulse generator module is configured as ssync master.

   a. Press Channel Select, 0, Config, and Indep (to set the mainframe Ssync bus). Press Channel Select, 1, Trig/Sync, and Master (to set the Channel 1 pulse generator as the ssync master).

   b. Verify a 1 kHz signal at J10 (SYS SYNC OUT) connector.

      (1) If there is no signal at J10, check the base input to Q3.

      (2) If the is a signal at the base of Q3, check the two differential pairs Q3/4 and Q1/2 and associated circuitry.

      (3) If there is no signal at the base of Q3, troubleshoot the input wiring from the base of Q3 to the SSYNC output of the 680-03 module.

2. Verify an output at J10 when an external ssync (J9) input is used as master.

a. Press Channel Select, 0, Config, Slave, Config, and Normal (to set the mainframe Ssync bus). Press Channel Select, 1, Trig/Sync, and Indep, Mode, Cont, Timing, Freq, 2, Exponent, 3, and execute (to set the Channel 1 pulse generator). Connect Pulse Out of the 680-03 module to the SYS SYNC IN connector (J9) of the VME Processor Board.

b. Verify a 2 kHz signal at J9 (SYS SYNC IN) and J10 (SYS SYNC OUT) connectors.

   (1) If there is no ssync signal at J10, check the base input to Q3.

   (2) If there is a signal at the base of Q3, check the two differential pairs Q3/4 and Q1/2 and associated circuitry.

   (3) If there is no ssync signal at the base of Q3, check the input pins (pins 5 and 7) of the TTL-to-ECL translator (U58).

   (4) If a ssync signal is present at U58-5, 7, check for the gate enable signal from U57-19 at U58-6. If missing, troubleshoot U57 and/or recheck menu setup. If present replace U58.

   (5) If the ssync signal is not present at U58-5 and 7, troubleshoot the input circuitry of R69, CR9 and 10, R70 and J9.

4.7.14 DFI Circuit Tests.

The DFI output should be open circuited during normal operation. Its operation is dependent on the real time clock 1 second interrupt produced by the VME 68000 microprocessor chip U1. It is reset to the open condition using the VME Processor Board Reset switch signal RESET/. Refer to schematic 1104-00-3904, sheet 5.

a. Remove power from the model 869. Use a DVM to check J8 for an open ciruit condition (normal).

b. If J8 is shorted, replace relay K1.

c. If J8 does not read shorted, remove the VME Processor Board. Install two extender cards (Wavetek P/N 1100-00-3212) and place the VME Processor Board on them. Power up the model 869.

d. Verify that TP55 (DFIHIT/) is a static TTL low. If not, check U56B. Press the VME Processor Board Reset switch. If TP55 goes TTL high, check Q5 and R58. If TP55 does not go high, check U55 and input signals (CSDFI/ and RESET/) to U56A.

4.8 UTILITY/GPIB DIAGNOSTIC ROUTINES (FUNCTION KEY F4 - DIAG)

The diagnostic routines controlled under the DIAG menu and its three sub-menus are for factory maintenance and test purposes only. They require specialized test setups and data not normally supplied to users. A portion of the diagnostic menu functions are used in paragraphs 4.6.2, 4.6.3, and 4.6.8 as required to perform Ref/Cal Board tests.

SECTION 5
PARTS AND SCHEMATICS

5.1 DRAWINGS

The following assembly drawings, parts lists, and schematics are in the arrangement shown below.

5.2 ERRATA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, errata pages are prepared to summarize the changes made and are inserted inside the shipping carton with this manual. If no such pages exist, the manual is correct as printed.

5.3 ORDERING PARTS

When ordering spare parts, please specify part number, circuit reference, board, serial number of unit and, if applicable, the function performed.

NOTE

An assembly drawing number is not necessarily the assembly part number. However, the assembly parts list number is the assembly part number

Drawing	Drawing No.
Model 869 Mainframe	
Schematic (2 shts)	1004-00-0641
Assembly (4 shts)	1101-00-3417
Parts List (2 shts)	1100-00-3417
Keyboard Display Board	
Schematic	0103-00-3124
Assembly	1100-00-3124
Parts List	1100-00-3124
I/O Processor Board	
Schematic (2 shts)	1104-00-3236
Assembly	1101-00-3236
Parts List	1100-00-3236
Main Interconnect Board	
Schematic (4 shts)	1104-00-3295
Assembly (2 shts)	1101-00-3295
Parts List	1100-00-3295
Reference/Calibrator Board	
Schematic (8 shts)	1104-00-3385
Assembly (2 shts)	1101-00-3385
Parts List (2 shts)	1100-00-3385
68000 VME Board	
Schematic (7 shts)	1104-00-3409
Assembly	1101-00-3409
Parts List (2 shts)	1100-00-3409

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REV	ECO	BY	DATE	APP
A	ERO 90-434	SC	7-9-90	

FRONT PANEL ASSEMBLY

DISPLAY BD ASSEMBLY
1100-00-3124

DISPLAY SUB ASSEMBLY
1206-00-2324

J3 P3: 1 RED, 2 N.C., 3 RED

J2 (33, 34) — P1 J1

I/O PROCESSOR BD.
1100-00-3236

A: 1, 32 J2 — B: 1, 32 J90

MAIN INTERCONNECT BD.
1100-00-

FAN SUB ASSEMBLIES
1206-00-2971

POWER STANDBY SWITCH
N.O. B
N.C.
N.O.
N.C. A

NOTE: WHEN POWER STANDBY SWITCH IS IN NORMALLY CLOSED POSITION, AS SHOWN, POWER SUPPLY IS NOT ACTIVATED

MJ2955 (E, B, C)

P41 J41: 1 BLK TEMP SENSOR, 2 WHT TEMP SENSOR, 3 RED TEMP SENSOR, 4 N.C., 5 N.C., 6 GRN +24V UNREG RET, 7 N.C., 8 YEL +24V UNREG, 9 N.C.

P40 J40: 1 BLK STANDBY SW, 2 WHT STANDBY SW

P27 J27 — J22 J19 J16 J13 J10 J7 J4 J1

P28 J28 — J23 J20 J17 J14 J11 J8 J5

68000 VME BD. 1100-00-3409

J2 J25 — J24 J21 J18 J15 J12 J9 J6

REF/CAL BD. 1100-00-3385

J1 J26

J32 P32: 9 -15V, 8 GND, 7 +5V, 6 +5V, 5 +5V, 4 +5V, 3 GND, 2 GND, 1 GND

J33 P33: 10 +15V, 9 -24V, 8 GND, 7 -5V, 6 N.C., 5 N.C., 4 N.C., 3 GND, 2 N.C., 1 N.C.

J34 P34: 8 GND, 7 GND, 6 GND, 5 GND, 4 ISO GND, 3 ISO +5V, 2 GND, 1 +24V

POWER SUPPLY
1204-00-2943

HEATSINK

VR4 −2V: OUT −2V, IN −5V, ADJ — J39 (3, 2, 1)

VR3 +5V: IN +5V, OUT +3V, ADJ — J38 (3, 2, 1)

VR2 −12V: OUT −12V, IN −15V, ADJ — J37 (3, 2, 1)

VR1 +12V: IN +15V, OUT +12V, ADJ — J36 (3, 2, 1)

Sys Sync In / Sys Sync Out / DPI

10 MHz Ref In / 10 MHz Ref Out / Sys Trig In / Sys Trig In / Digital Scan In / Cal In

GRN/YEL, GRAY, RED, BLK, WHT, GRN/YEL

SW1 — GPIB — FI — HOT, NEUT, GND

GPIB ADDRESS SWITCH

115V/230V VOLTAGE SELECT SWITCH (SHOWN IN 115V POSITION)

A.C. POWER SWITCH

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DO NOT SCALE DRAWING

DRAWN	CHERMACK	6-4-90
CHECKED	N. C. Nulk	7/1/90
PROJ. ENGR	Kwok Lo	7-13-90
RELEASE APPROV	Kwok Lo	7-13-90

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: SCHEMATIC, INSTRUMENT

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1004-00-0641	A

SCALE NONE | MODEL 869 | SHEET 1 OF 2

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REV	ECO	BY	DATE	APP

SYNC OUT
(50 OHM)
TRIG IN
(50 OHM)
PULSE OUT
(50 OHM)
1200-00-3253
REAR END CAP ASSY.

1100-00-3418

P20 J20
P25 J25

1100-00-3271
PCA TIMING BD.

1100-00-3130
VCO ASSEMBLY
DCVIN 1
GND 2
SIGOUT 3
V+ 4

P7 J7: GND GND PRETRIG GND GND GND HPULSB GND HPULSA GND
P6 J6: GND -15V +15V -5V +5V GND VBB GND T10MHZ GND GND SSYNC +24V -5V +5V SYNC-T STRIG GND CLKM CLKD
P5 J5: GND N/C XTLEVEL VDLY VPLSMD N/C +5V N/C LD3 LD2 LD1 LD0 GND GND LA17 LA16 LA15 N/C N/C +5V N/C N/C LRESET CS2 LDS GND

J13 P13

1100-00-3250
HYBRID HEATSINK
MODULE ASSY.

P10 / J10 / J4 (TEST CONN.)

	P10	J10	J4
20	GND	20	18
19	-13VF	19	17
18	IAMPL	18	16
17	RAMP4	17	15
16	RAMP3	16	14
15	RAMP2	15	13
14	N/C	14	12
13	-IR	13	11
12	-8VF	12	10
11	HPULSB	11	9
10	HPULSA	10	8
9	VOF	9	7
8	+13VF	8	6
7	+IR	7	5
6	+5V	6	4
5	N/C	5	3
4	IT	4	2
3	VCC	3	1
2	VT	2	
1	GND	1	

E1 P9 J9 AUTOCAL

J14 P14
VRELAY
RCALOUT
R4XATT
R2XATT
P8 J8

1100-00-3273
PCA OUTPUT BD.

P3 P2 P1

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 6-8-90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: INSTRUMENT SCHEMATIC
	ENGR. ENGR		
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1004-00-0641 · REV A · SCALE NONE · MODEL 869 · SHEET 2 OF 2

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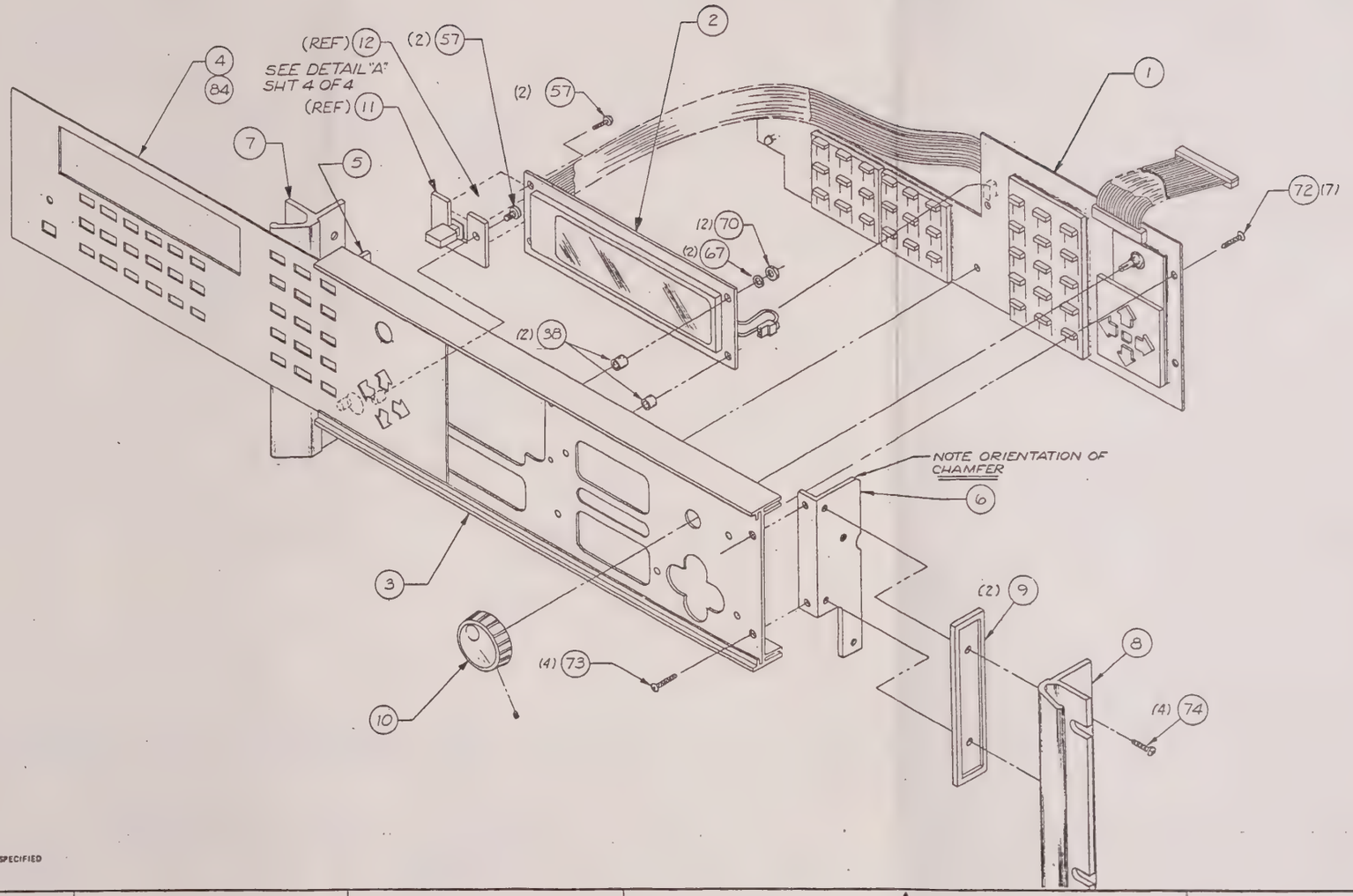

NOTE: UNLESS OTHERWISE SPECIFIED

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MATERIAL —	PROJ ENG'R Chuck Ho 7-9-90		TITLE ASSEMBLY, CHASSIS
	RELEASE APPROV Chuck Ho		
FINISH WAVETEK PROCESS —	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 869 / DWG NO. 1101-00-3417 / REV A
	SCALE NONE		CODE IDENT. 23338 / SHEET 1 OF 4

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A27086

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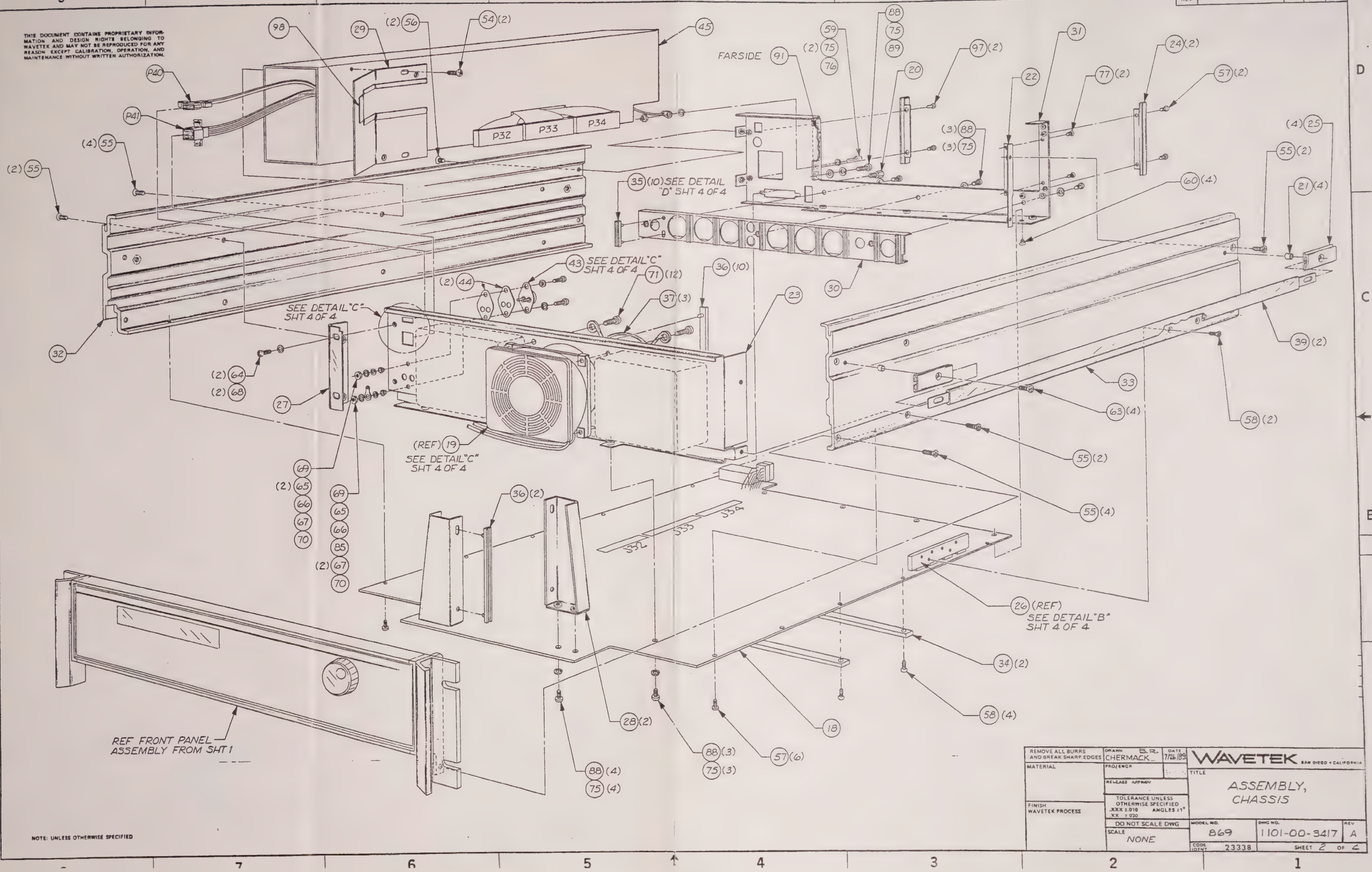
REV	ECN	BY	DATE	APP



NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B.R. CHERMACK	DATE 7/26/89	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: ASSEMBLY, CHASSIS
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 869 / DWG NO. 1101-00-3417 / REV A
	SCALE NONE		CODE IDENT 23338 / SHEET 2 OF 4

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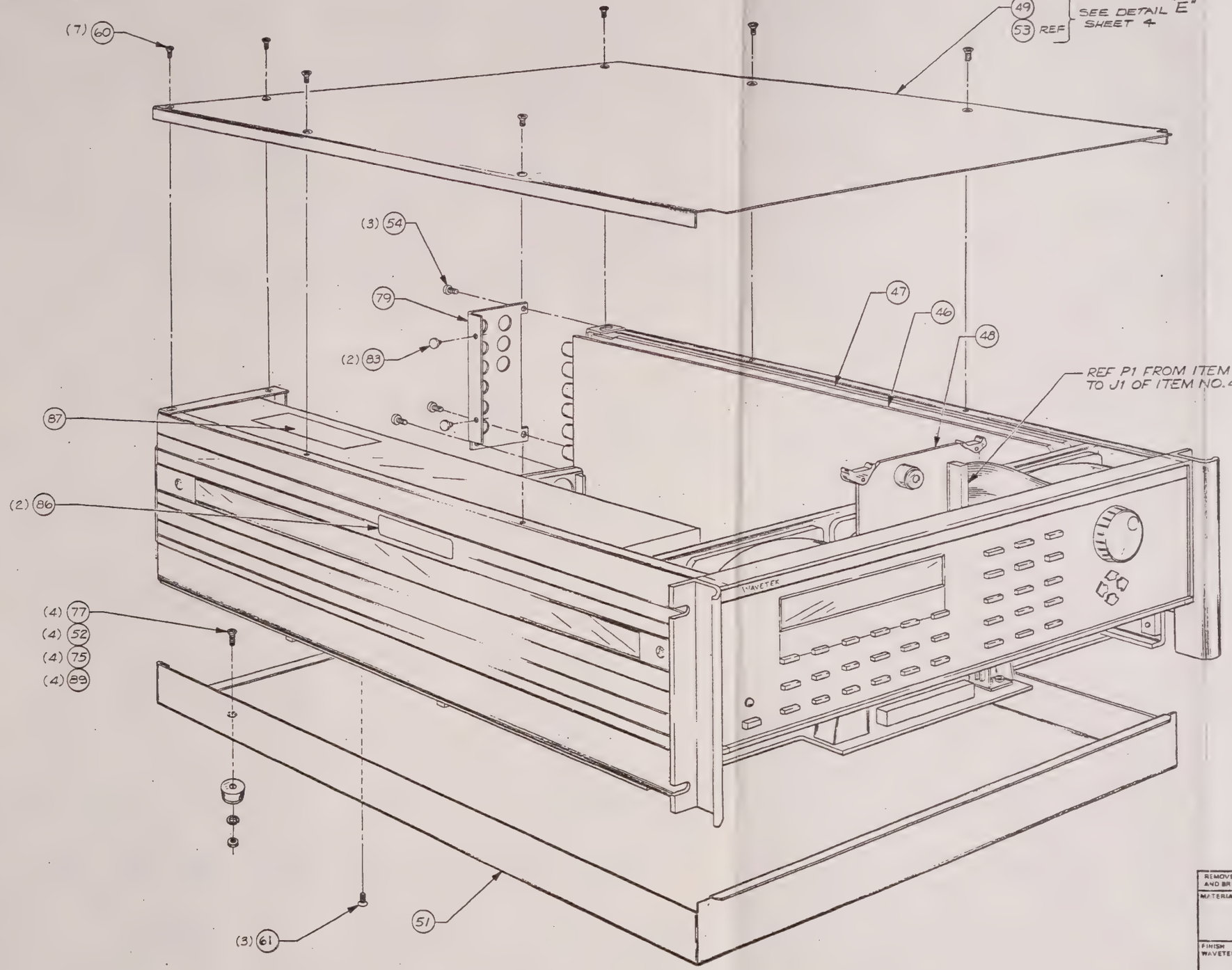
REV	ECN	BY	DATE	APP



NOTE: UNLESS OTHERWISE SPECIFIED.

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN B.R. CHERMACK	DATE 7/24/89	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: ASSEMBLY CHASSIS
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG	MODEL NO. 869	DWG NO. 1101-00-3417 REV A
	SCALE NONE	CODE IDENT 23338	SHEET 3 OF 4

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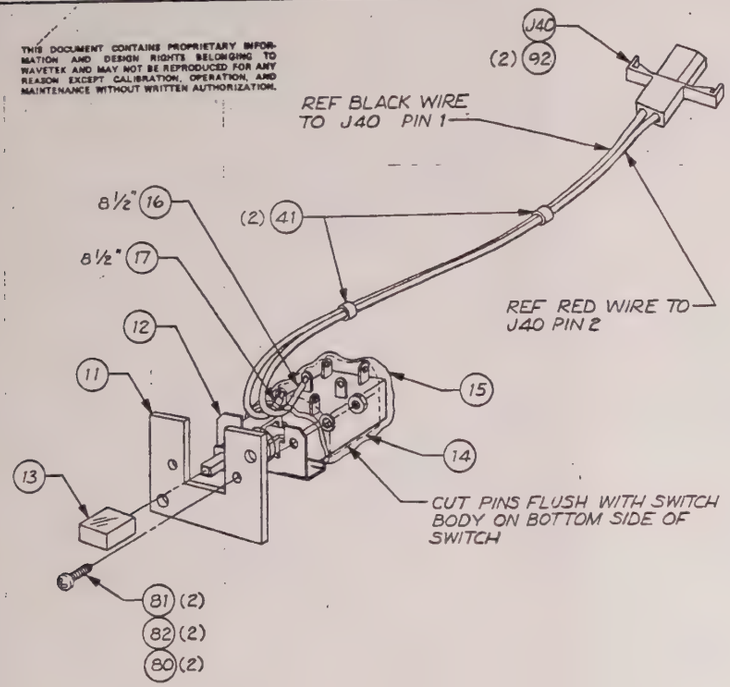
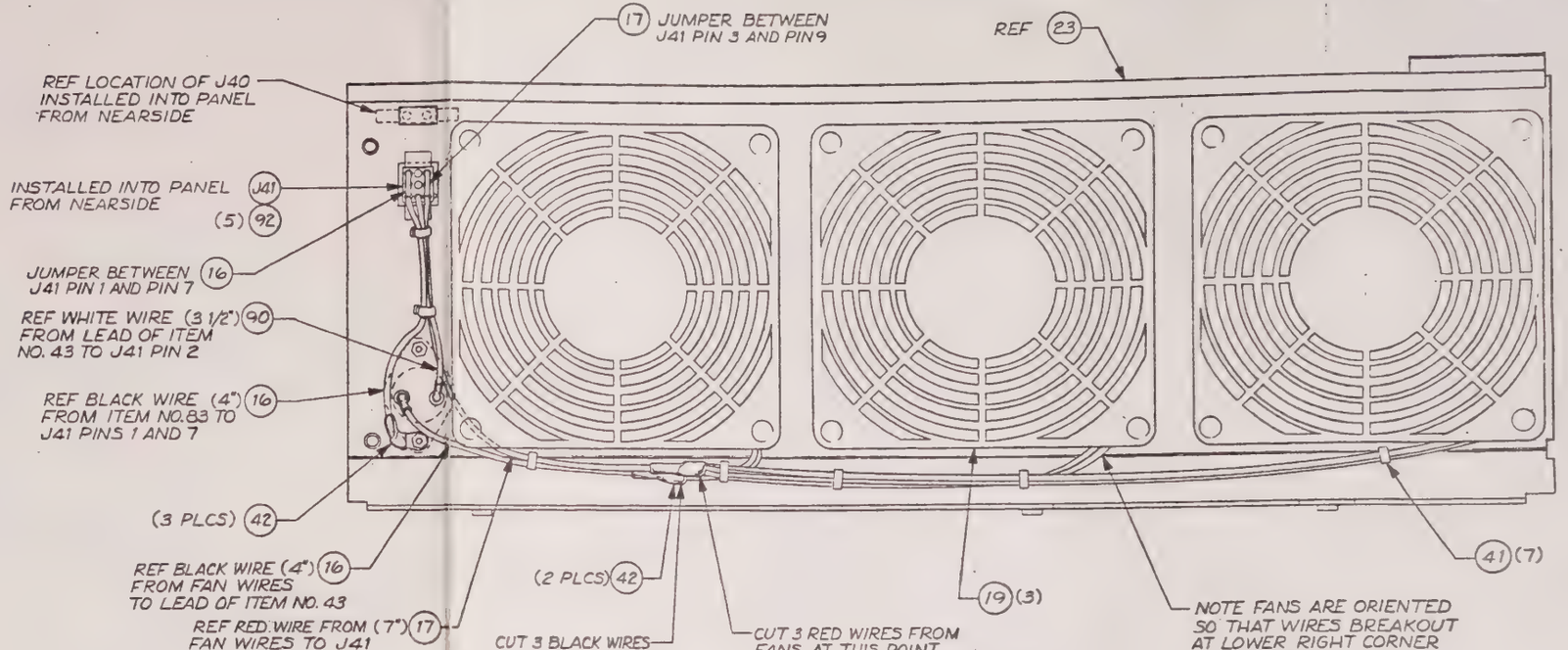


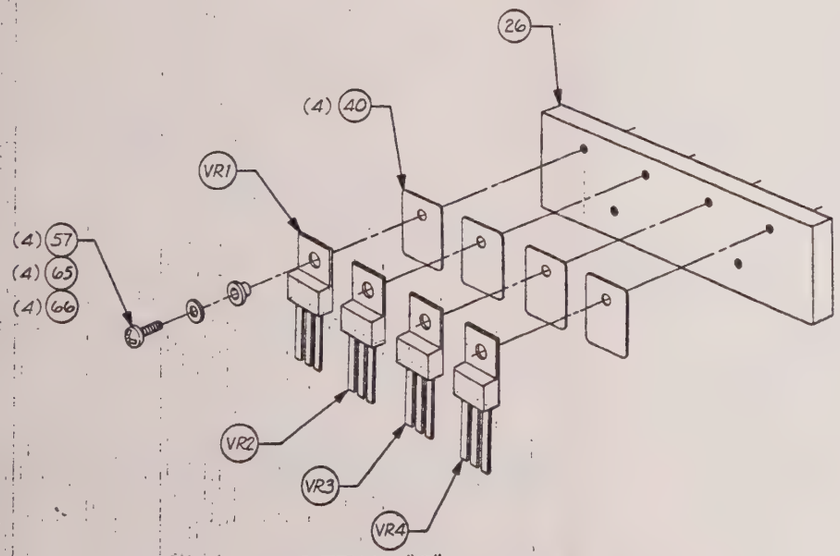
DETAIL "A"

SWITCH ASSEMBLY AND WIRING


17 JUMPER BETWEEN J41 PIN 3 AND PIN 9
REF 23
REF LOCATION OF J40 INSTALLED INTO PANEL FROM NEARSIDE
INSTALLED INTO PANEL FROM NEARSIDE
J41
(5) 92
JUMPER BETWEEN J41 PIN 1 AND PIN 7
16
REF WHITE WIRE (3 1/2") FROM LEAD OF ITEM NO. 43 TO J41 PIN 2
90
REF BLACK WIRE (4") FROM ITEM NO. 83 TO J41 PINS 1 AND 7
16
(3 PLCS) 42
REF BLACK WIRE (4") 16 FROM FAN WIRES TO LEAD OF ITEM NO. 43
REF RED WIRE FROM (7") 17 FAN WIRES TO J41 PINS 3 AND 9
(2 PLCS) 42
CUT 3 BLACK WIRES AT THIS POINT, AND REPEAT THE SAME PROCESS AS ON RED WIRES BUT TWIST TOGETHER WITH BLK WIRE.
CUT 3 RED WIRES FROM FANS AT THIS POINT. CUTBACK INSULATION APPROX 1/2", TWIST TOGETHER WITH ITEM NO. 17 SOLDER AND INSULATE WITH ITEM NO. 42
19 (3)
NOTE FANS ARE ORIENTED SO THAT WIRES BREAKOUT AT LOWER RIGHT CORNER ON ALL 3 FANS.
41 (7)

DETAIL "C"

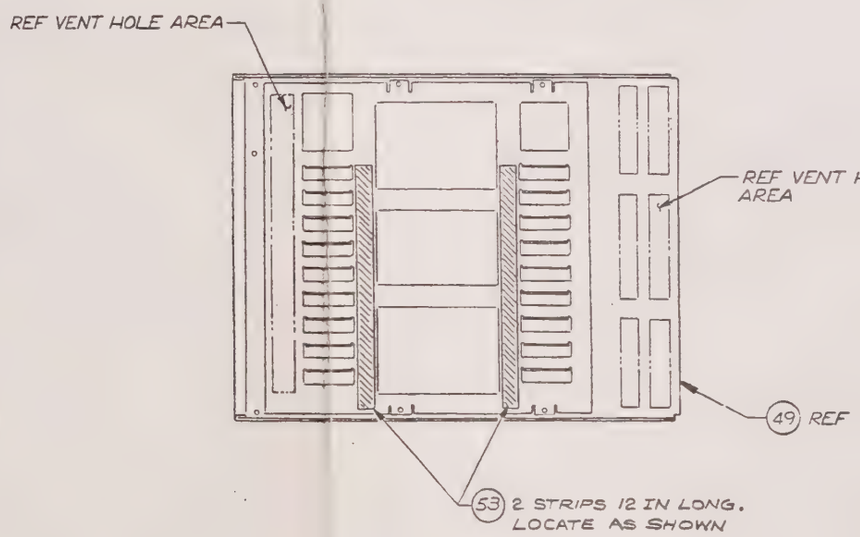
INSTALLATION AND WIRING OF FANS



DETAIL "B"

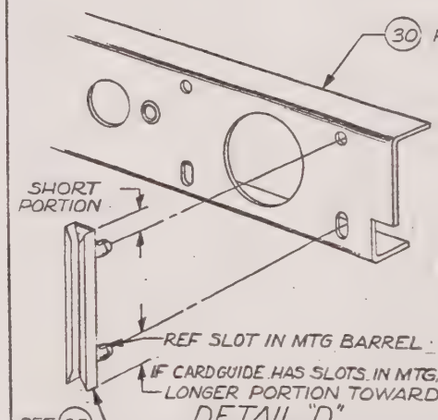
VOLTAGE REGULATOR TO HEATSINK INSTALLATION

NOTE: UNLESS OTHERWISE SPECIFIED



DETAIL "E"

TOP COVER ASSEMBLY


30 REF
SHORT PORTION
REF SLOT IN MTG BARREL
IF CARDGUIDE HAS SLOTS IN MTG. BARRELS, LOCATE LONGER PORTION TOWARDS BOTTOM, 10 PLCS
REF 35

DETAIL "D"

CARDGUIDE ORIENTATION

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK B.R.	DATE 7/24/89	WAVETEK SAN DIEGO, CALIFORNIA	
MATERIAL	PROJ ENGR		TITLE ASSEMBLY, CHASSIS	
	RELEASE APPROV			
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030			
	DO NOT SCALE DWG		MODEL NO. 869	DWG NO. 1101-00-3417 REV A
	SCALE		CODE IDENT 23338	SHEET 4 OF 4

REV	ECN	BY	DATE	APP

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REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	AUTOMATIC TEST PROCEDURE	0003-00-0545	WVTK	0003-00-0545	1
NONE	OUTLINE DRAWING-INSTR	0009-00-0545	WVTK	0009-00-0545	1
NONE	ACCEPTANCE TEST PROCEDURE-869	1002-00-0641	WVTK	1002-00-0641	1
NONE	PCA, DISPLAY BD	1100-00-3124	WVTK	1100-00-3124	1
18	MAIN INTERCONNECT BOARD	1100-00-3295	WVTK	1100-00-3295	1
46	PCA, REF CAL BOARD	1100-00-3385	WVTK	1100-00-3385	1
47	PCA, VME BD	1100-00-3409	WVTK	1100-00-3409	1
NA	PCA, PROCESSOR BD	1100-00-3626	WVTK	1100-00-3626	1
NONE	A/D CHASSIS-869	1101-00-3417	WVTK	1101-00-3417	1
10	ASSY ENCODER KNOB	23-1731	WVTK	1201-00-1731	1
45	POWER SUPPLY, 680	1204-00-2943	XENTK	1204-00-2943	1
2	ASSY, SUB-ASSY DISPLAY	630-2324	WVTK	1206-00-2324	1
19	SUB-ASSEMBLY, FAN	1206-00-2971	WVTK	1206-00-2971	3
14	INSULATOR, PWR SWITCH REF: 1600-99-0001	801-8370	WVTK	1400-00-8370	1

WAVETEK PARTS LIST | TITLE CHASSIS ASSY-869 | ASSEMBLY NO. 1100-00-3417 | REV H | PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
11	BRACKET, POWER SWITCH MOUNTING	650-9363	WVTK	1400-01-9363	1
21	BUSHING, CARRYING STRAP	6787-M10-F05-I	UNICP	1400-01-9383	4
86 NONE	LABEL, WEIGHT WARNING			1400-02-0160	2
87	LABEL, WARNING: HAZARDOUS VOLTAGES	650-0760	WVTK	1400-02-0760	1
23	BRACKET, FAN & CARD GUIDE	1400-02-2653	WVTK	1400-02-2653	1
25	CAP, CARRYING STRAP	1400-02-2732	WVTK	1400-02-2732	4
26	HEATSINK, VOLTAGE REGULATOR	1400-02-2763	WVTK	1400-02-2763	1
27	BRACKET, MOUNTING, FAN WALL	1400-02-2813	WVTK	1400-02-2813	1
9	VERTICAL CORNER TRIM	1400-02-2841	WVTK	1400-02-2841	2
8	HANDLE, RACKEAR, RIGHT	1400-02-2852	WVTK	1400-02-2852	1
7	HANDLE, RACKEAR, LEFT	1400-02-2862	WVTK	1400-02-2862	1
28	MICROPROCESSOR, CARD SUPPORT	1400-02-2873	WVTK	1400-02-2873	2
29	POWER SUPPLY AIRFLOW BAFFLE	1400-02-2893	WVTK	1400-02-2893	1

WAVETEK PARTS LIST | TITLE CHASSIS ASSY-869 | ASSEMBLY NO. 1100-00-3417 | REV H | PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
5	CORNER BRACKET, LEFT	1400-02-2913	WVTK	1400-02-2913	1
6	CORNER BRACKET, RIGHT	1400-02-2923	WVTK	1400-02-2923	1
30	BRACKET, CARD GUIDE, REAR PANEL	1400-02-2934	WVTK	1400-02-2934	1
3	SUB-PANEL, FRONT	1400-02-3012	WVTK	1400-02-3012	1
34	STIFFENER, MOTHER BD-680	1400-02-3120	WVTK	1400-02-3120	2
49	COVER ASSY, TOP	1400-02-4997	WVTK	1400-02-4997	1
22	BRACKET, MOUNTING, REAR PANEL	1400-02-5008	WVTK	1400-02-5008	1
79	DRESS PANEL REAR			1400-02-5009	1
31	REAR PANEL	1400-02-5012	WVTK	1400-02-5012	1
51	COVER, BOTTOM	1400-02-5013	WVTK	1400-02-5013	1
32	SIDE PANEL, LEFT	1400-02-5014	WVTK	1400-02-5014	1
33	SIDE PANEL, RIGHT	1400-02-5015	WVTK	1400-02-5015	1
24	TRIM CAP, SIDE	1400-02-5016	WVTK	1400-02-5016	2
4	DRESS FRONT PANEL, 869	1400-02-5094	WVTK	1400-02-5094	1
53	TAPE, CLSED CELL	4516	3M	1600-02-0016	24

WAVETEK PARTS LIST | TITLE CHASSIS ASSY-869 | ASSEMBLY NO. 1100-00-3417 | REV H | PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	NEOPRENE SPNGE TPE 1/16X1IN.				
J41	CONN, 9PIN	03-06-1091	MOLEX	2100-02-0010	1
J40	CONN, RECPT, .062 PDS, W/DET & MT EAR	03-06-1022	MOLEX	2100-02-0083	1
85	SOLDER LUG	11A144	ZIER	2100-04-0025	1
92	PIN, FEMALE	350628-1	AMP	2100-05-0002	7
35	CARD GUIDE-650	2100-06-0019	WVTK	2100-06-0019	10
36	CARD GUIDE, 680	N-350-2	BIVAR	2100-06-0023	12
20	HARDWARE KIT, GPIB CONN	554808-1	AMP	2100-07-0024	1
NONE	FUSE, 12A, 250V.	MDA-12	BUSMN	2400-05-0057	1
37	FINGER GUARD	055012	HANSU	2600-01-0007	3
41	TY-WRAP	TY-523M	TB	2800-00-0006	9
38	SPACER .187H .187 DIA .115 DIA THRU	8-1101-.115-3	GLOBE	2800-04-0021	2
39	CARRYING STRAP	2800-07-0031	WVTK	2800-07-0031	2
52	FOOT, RUBBER	2197W	ROYAL	2800-08-0013	4
83	FASTENER, SPLIT STEM,	138-NN-5426	PLACO	2800-09-0044	2

WAVETEK PARTS LIST | TITLE CHASSIS ASSY-869 | ASSEMBLY NO. 1100-00-3417 | REV H | PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
	DOMED HD				
65	WASHER	5607-150	SESTM	2800-11-0015	7
80	NUT, HEX, 2-56, Z	2-56 HEX NUT	CMRCL	2800-14-2100	2
76	NUT, FLEXLOC, 6-32, Z	6-32 NUT F.L.	CMRCL	2800-15-6100	1
70	NUT, HEX, 4-40 R/P, Z	4-40 R/P	CMRCL	2800-16-4100	4
58	SCREW, 4-40X7/16, FHP, 82 DEG, Z	4-40X7/16 FH	CMRCL	2800-19-4107	6
97	SCREW, 4-40X3/16, PHP, NYLOK PATCH	4-40 X 3/16	CMRCL	2800-23-4103	2
57	SCREW, 4-40X1/4, PHP, NYLOK PATCH, Z 4-40X1/4	4-40 X 1/4	CMRCL	2800-23-4104	16
72	SCREW, 6-32X1/4, PHP, Z NYLOK PELLET	6-32 X 1/4	CMRCL	2800-23-6104	7
54	SCREW, 6-32X5/16 PHP, NYLOK PATCH, Z PATCH, 6-32 X 5/16	6-32X 5/16 NYLOK	CMRCL	2800-23-6105	5
59	SCREW, 6-32X1/2, SOC CAP, Z	6-32X1/2 SKT CAP	CMRCL	2800-23-6108	1
66	WASHER, FLAT, #(.209 O.D.)	NAS620-4	CMRCL	2800-26-4001	6
89	WASHER, FLAT, #6 BIN	#6FLAT WASHER	CMRCL	2800-26-6001	3

WAVETEK PARTS LIST | TITLE CHASSIS ASSY-869 | ASSEMBLY NO. 1100-00-3417 | REV H | PAGE 5

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	495				
81	SCREW, PAN, CAD I, CROSS RECESS, 2-56 X 1/4	MS51957-3	COML	2800-38-2104	2
69	SCREW, PAN, CAD I, CROSS RECESS, 4-40 X 1/2	MS51957-17	COML	2800-38-4108	2
88	SCREW, 6-32X3/8 PHP, Z	MS51957-28	COML	2800-38-6106	11
71	SCREW, 6-32X3/4 PHP, Z 6-32 X 3/4	6-32 X 3/4 PAN	CMRCL	2800-38-6112	12
64	SCREW, PAN, CAD I, CROSS RECESS, 8-32 X 3/8	8-32 X 3/8 PAN	CMRCL	2800-38-8106	2
82	#2 LOCKWASHER, PLATED	#2SRLW	CMRCL	2800-42-2000	2
67	#4 LOCKWASHER, PLATED	#4SRLW	CMRCL	2800-42-4000	5
75	#6 LOCKWASHER, PLATED	#6SRLW	CMRCL	2800-42-6000	17
68	LOCKWASHER, #8 SPLIT RING, SS	#8SRLW	CMRCL	2800-42-8000	2
60	SCREW, 6-32X1/4 FH PHLP 100 BLK OX.	6-32 X 1/4 FH, 100	CMRCL	2800-43-6104	11
77	SCREW, 6-32X3/8 FH 100 PHLP, Z 6-32 X 3/8	6-32 X 3/8 F.H. 100	CMRCL	2800-44-6106	6

WAVETEK PARTS LIST | TITLE CHASSIS ASSY-869 | ASSEMBLY NO. 1100-00-3417 | REV H | PAGE 6

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES | MATERIAL | FINISH WAVETEK PROCESS | DO NOT SCALE DRAWING

DRAWN | DATE | CHECKED | PROJ. ENGR. | RELEASE APPROV

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± XX ± XXX ± ±

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: PARTS LIST MODEL 869 MAINFRAME

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1100-00-3417	H

SCALE | MODEL 869 | SHEET 1 OF 2

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REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
73	SCREW, PLPS, FLAT, CAD I, 100DEG, 8-32X3/8	8-32X3/8	CMRCL	2800-44-8106	4
74	SCREW, PLPS, FLAT, CAD I, 100DEG, 8-32X5/8	8-32X5/8	CMRCL	2800-44-8110	4
63	SCREW, 10-32X7/16 FH PHLP 100 BLK OX.	2800-51-0107	CMRCL	2800-51-0107	4
61	SCREW, PHLP, 6-32X3/16, 100 DEG, BLK OX.	6-32X3/16, 100 DEG, BLK	CMRCL	2800-51-6103	6
56	SCREW, 8-32X1/4 FH PHLP 82, BLK OX.	2800-55-8104	CMRCL	2800-55-8104	2
55	SCREW, 8-32X3/8 FH PHLP 82, BLK OX	2800-55-8106	CMRCL	2800-55-8106	14
98	RUBBER SEAL	447	ACCUR	3000-00-0005	.5
NONE	COONTAINER, 23 X 27 X 12 FOR 680	101-20A	HIGH	3000-00-0193	1
NONE	INSERT , FOAM, FOR 680	101-20	HIGH	3000-00-0194	1
NONE	CARTON, ACCESSORY, 11 X 20 X 1 FOR 680	101-20B	HIGH	3000-00-0195	1
44	INSULATOR(TO-3)	7403-09FR-05	BERQG	3100-00-0011	2
40	THERMAL CONDUCTIVE INSULATOR, TO-220	173-7-240A	WAKE	3100-00-0014	4

WAVETEK PARTS LIST	TITLE CHASSIS ASSY-869	ASSEMBLY NO. 1100-00-3417	REV H
		PAGE 7	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
43	TRANS, PWR, SILICON, PNP	MJ2955	MOT	4902-29-5500	1
12	SWITCH ASSY PB	5103-00-0020	WVTK	5102-00-0005	1
90	WIRE, MU, 20GA, WHITE	H0101018 (WHT)	JUDD	6000-32-0009	5
16	WIRE, MU, 22GA	H0101029 (BLK)	JUDD	6000-32-2000	3
17	WIRE, MU, 22GA, TINNED COPPER	780-22 (RED)	ATLAS	6000-32-2002	3
42	SHRINK TUBING, 1/8 IN	FIT-221-1/8	ALPHA	6001-20-2000	3
15	SHRINK, CLEAR 1	FP-301-1	ELCHC	6001-21-6000	.3
VR1 VR3	VOLT REGULATOR, 3 TERMINAL ADJUSTABLE POS	LM317T	NSC	7000-03-1700	2
VR2 VR4	VOLT REGULATOR	LM337T	NSC	7000-03-3700	2

WAVETEK PARTS LIST	TITLE CHASSIS ASSY-869	ASSEMBLY NO. 1100-00-3417	REV H
		PAGE 8	

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE
	PROJ. ENGR.		PARTS LIST MODEL 869 MAINFRAME
FINISH WAVETEK PROCESS	RELEASE APPROV.		
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± .XXX ± ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1100-00-3417 · REV H
DO NOT SCALE DRAWING			SCALE · MODEL 869 · SHEET 2 OF 2

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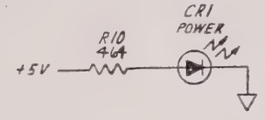
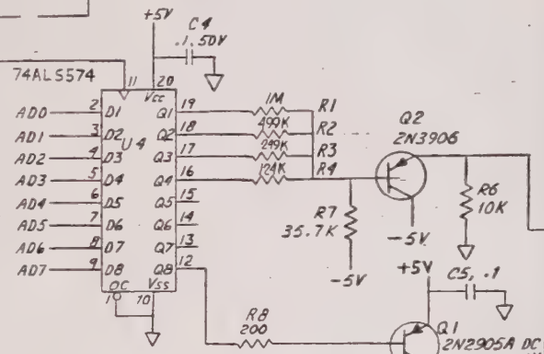
REV	ECN	BY	DATE	APP
A	ERO 9801	RO	5-20-88	E.R.

ADDRESS DECODER

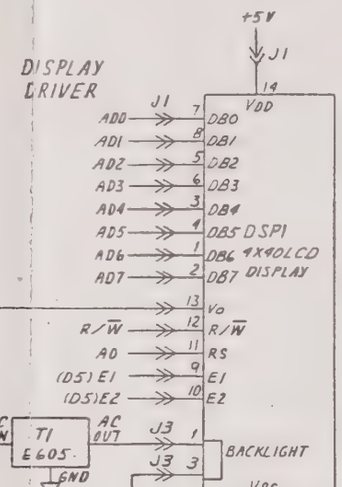


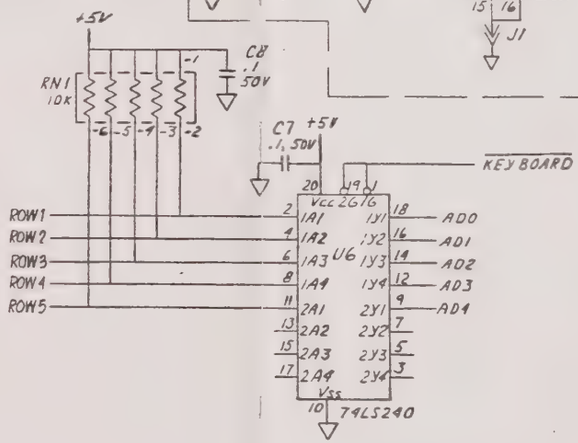
DC to DC CONVERTER

DIAL ENCODER



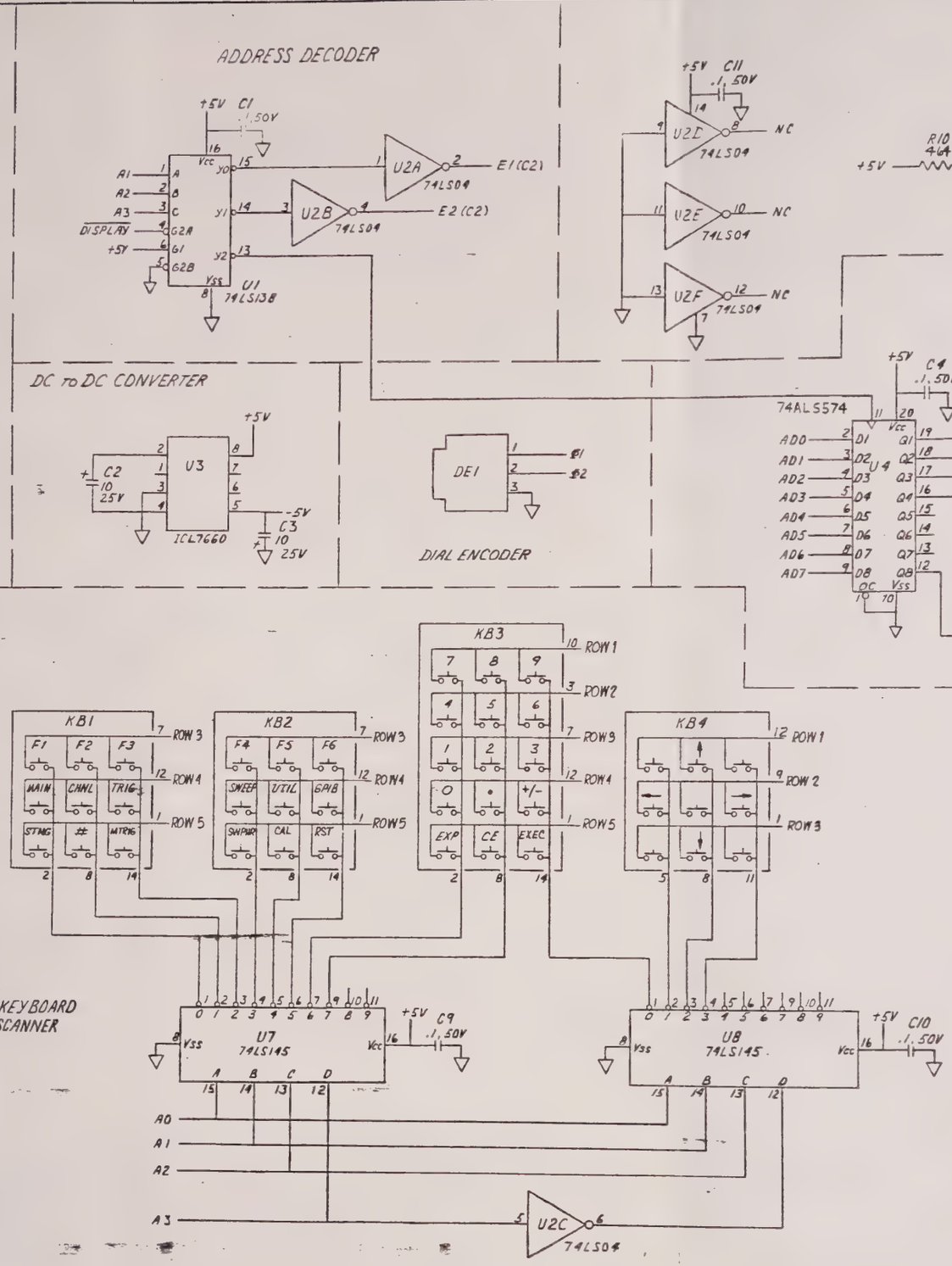
DISPLAY DRIVER

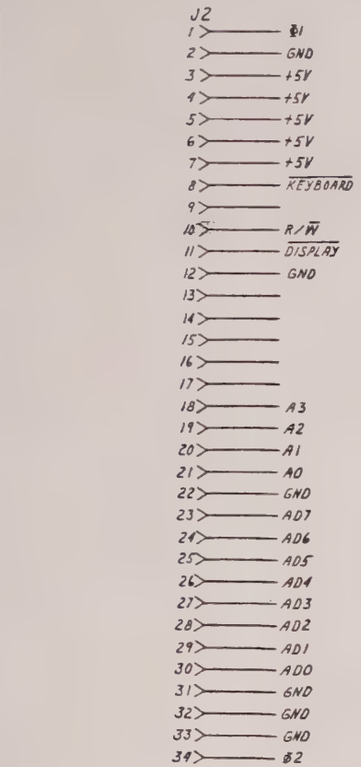




KEYBOARD READ BUFFER

KEYBOARD SCANNER





4. ALL CAPACITORS ARE IN MICROFARADS.
3. ALL RESISTERS ARE IN OHMS, 1%, 1/8W.
2. ALL +5V AND ⏚ ARE ISO.
1. ALL KEYBOARDS NUMBERED FROM THE TOP.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN RO FIFER 5-20-88
PROJENGR Ed Ramos 6/88
RELEASE APPROVED Ollie Hilleto
TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ± .010 ANGLES ± 1° .XX ± .030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE
SCHEMATIC
KEYBOARD / DISPLAY

MODEL NO. 680
DWG NO. 0103-00-3124
REV A
CODE IDENT 23338
SHEET / OF /

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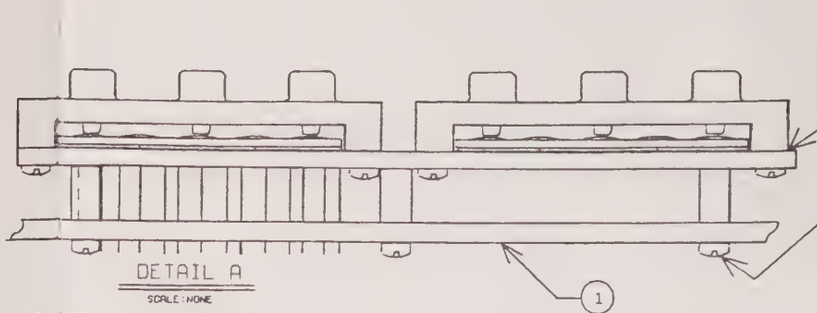
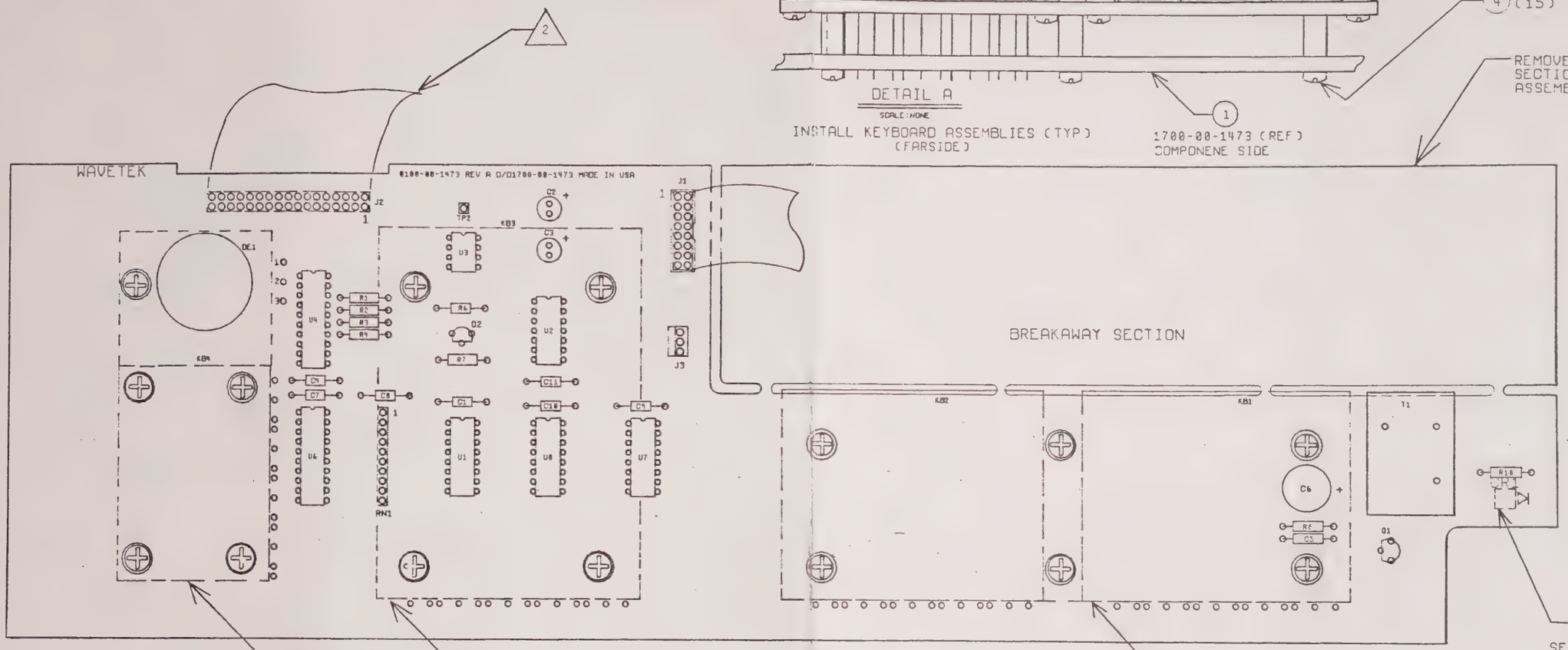
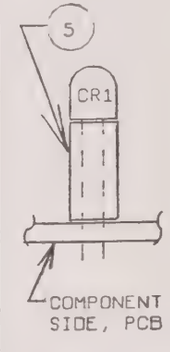
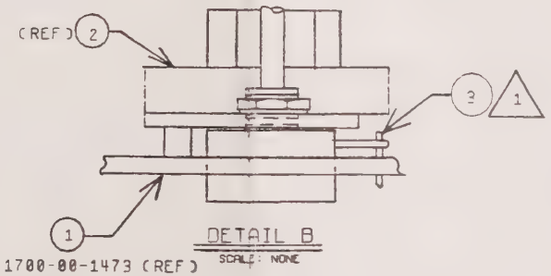
REV	ECN	BY	DATE	APP
A	ERO 9801	RO	5-88	[illegible]









WIRE LIST			
FROM	TO	GAUGE	LENGTH
DE1-1	1	22 BUS	3/8IN
DE1-2	2	22 BUS	3/8IN
DE1-3	3	22 BUS	3/8IN

2. INSTALL ITEMS IN PHANTOM LINES ON FAR SIDE OF PCB.

1. SOLDER TO PCB PER WIRE LIST, ON FARSIDE OF PCB

UNLESS OTHERWISE SPECIFIED

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN RO FIFER
DATE
PROVENCE Ed Kenon
RELEASED
TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE ASSEMBLY DRWG FRONT PANEL PCB

MODEL NO.	DWG NO.	REV
680	1100-00-3124	A

CODE IDENT 23338 SHEET 1 OF 1

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REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
	LOCK PATCH, Z 4-40X1/4				
S	SPACER NYLON L.E.D.	905-500	BIVAR	3000-00-0106	1
R6	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	1
R1	RES, MF, 1/8W, 1%, 1M	RN55D-1004F	TRW	4701-03-1004	1
R4	RES, MF, 1/8W, 1%, 124K	RN55D-1243F	TRW	4701-03-1243	1
R8	RES, MF, 1/8W, 1%, 200	RN55D-2000F	TRW	4701-03-2000	1
R3	RES, MF, 1/8W, 249K	RN55D-2493F	TRW	4701-03-2493	1
R7	RES, MF, 1/8W, 1%, 35.7K	RN55D-3572F	TRW	4701-03-3572	1
R10	RES, MF, 1/8W, 1%, 464	RN55D-4640F	TRW	4701-03-4640	1
R2	RES, MF, 1/8W, 1%, 499K	RN55D-4993F	TRW	4701-03-4993	1
RN1	RES NETWORK 10K 2% 10PIN SIP BUSS	4310R-101-103	BOURN	4770-00-0008	1
CR1	LED, GREEN	XC5560	X-CIT	4899-00-0021	1
Q1	TRANS 2N2905A PNP GENERAL PURPOSE TO-5	2N2905A	MSC	4901-02-9051	1
Q2	TRANS 2N3906 PNP GENERAL PURPOSE TO-92	2N3906(OBS)	FAIR	4901-03-9060	1
T1	TRANSFORMER	E605-E0003	ENDRE	5600-00-0032	1

WAVETEK PARTS LIST	TITLE PCA, DISPLAY BD	ASSEMBLY NO. 1100-00-3124	REV A
		PAGE 2	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, DISPLAY BD	0103-00-3124	WVTK	0103-00-3124	1
7	ASSY, KEYTOP SUB-ASSY (3X6)	630-2040	WVTK	1206-00-2040	1
6	ASSY, KEYTOP SUB-ASSY (5X3)	630-2041	WVTK	1206-00-2041	1
2	ASSY, KEYTOP SUB-ASSY (CURSOR)	630-2323	WVTK	1206-00-2323	1
C1 C10 C11 C4 C5 C7 C8 C9	CAP, CER, MON, .1MF, 50V, AXIAL	CAC03Z5U104Z050A	CORNC	1500-01-0405	8
C2 C3	CAP, ELECT, 10MF/25V RADIAL LEAD, SP .10	NRE 10/63	NIC	1500-31-0002	2
C6	CAP, ELECT, 1000MF/16V RADIAL LEAD, SP .20	1500-31-0214	WVTK	1500-31-0211	1
1	DRILL DRWG, DISPLAY BD REF: SPEC 0008-00-0455 REV E	1700-00-1473	WVTK	1700-00-1473	1
J3	CONN, HEADER, RT ANG, MTA 100, 3POS, FRCTN LK	640457-3	AMP	2100-02-0248	1
TP2	TEST POINT, PC-TYPE	2100-04-0055	WVTK	2100-05-0024	1
8	TRANSIPAD	10123N(OBS)	METRS	2800-11-0003	1
4	SCREW, 4-40X1/4, PHP, NY	4-40 X 1/4	CMRCL	2800-23-4104	15

WAVETEK PARTS LIST	TITLE PCA, DISPLAY BD	ASSEMBLY NO. 1100-00-3124	REV A
		PAGE 1	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
3	BUSS WIRE, 22GA	298	ALPHA	6000-92-2000	1
J1	ASSY, RIBBON CABLE	6002-00-0031	WVTK	6002-00-0031	1
J2	ASSY RIBBON CABLE	6002-00-0032	WVTK	6002-00-0032	1
U2	INVERTER, HEX, TTL LOW PWR SCHTTKY	SN74LS04N	TI	8000-74-0410	1
U3	CONVERTER, SWITCH CAP VOLT, CMOS	ICL7660CPA	INTSL	8000-76-6000	1
U1	DECODER, 1-8 LINE, TTL	74LS138	TI	8007-41-3810	1
U7 U8	CDDR/DRV, BCD-DEC, TTL	74LS145	SIG	8007-41-4510	2
U6	BUF, OCT 3ST OUT, TTL	M74LS240P	MITSU	8007-42-4010	1
U4	FLIP-FLOP, OCTAL D	SN74ALS574N	TI	8007-45-7450	1

WAVETEK PARTS LIST	TITLE PCA, DISPLAY BD	ASSEMBLY NO. 1100-00-3124	REV A
		PAGE 3	

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK San Diego, California
MATERIAL	CHECKED		TITLE: PARTS LIST KEYBOARD DISPLAY BOARD
	PROJ. ENGR.		
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO 23338 · DWG NO. 1100-00-3124 · REV A · SCALE · MODEL 869 · SHEET 1 OF 1

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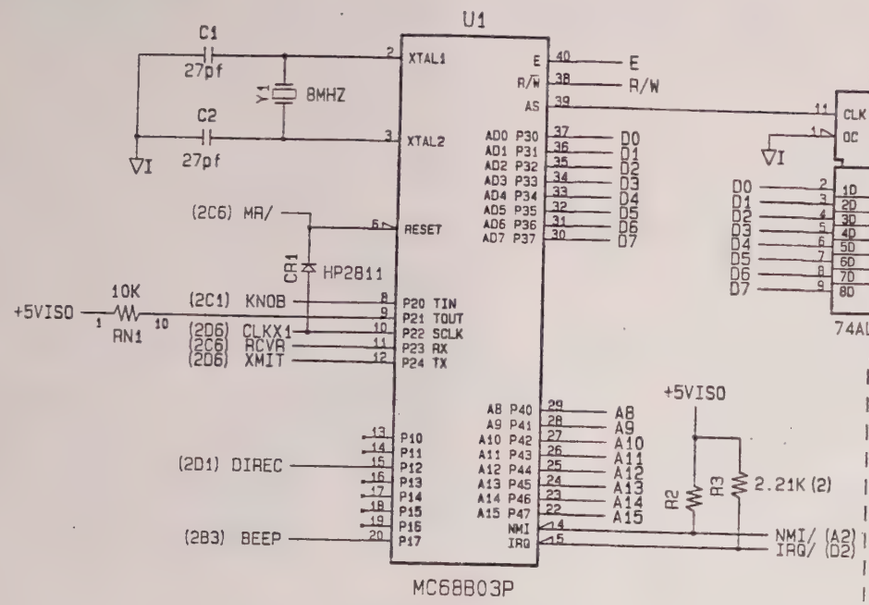
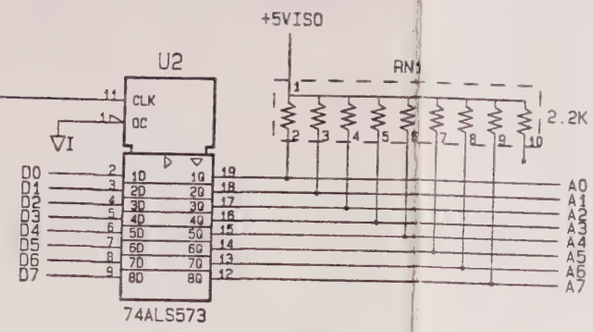
REV	ECN	BY	DATE	APP
A	ECO # 89-211	DB	5/14/89	
B	ECO # 90-288	MS	3/7/90	DD

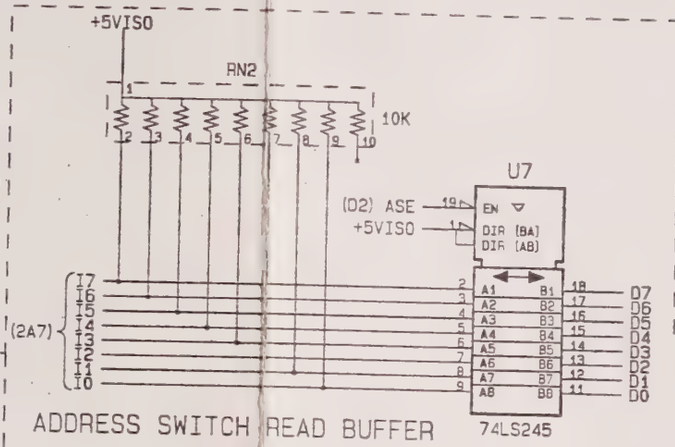
MICROPROCESSOR



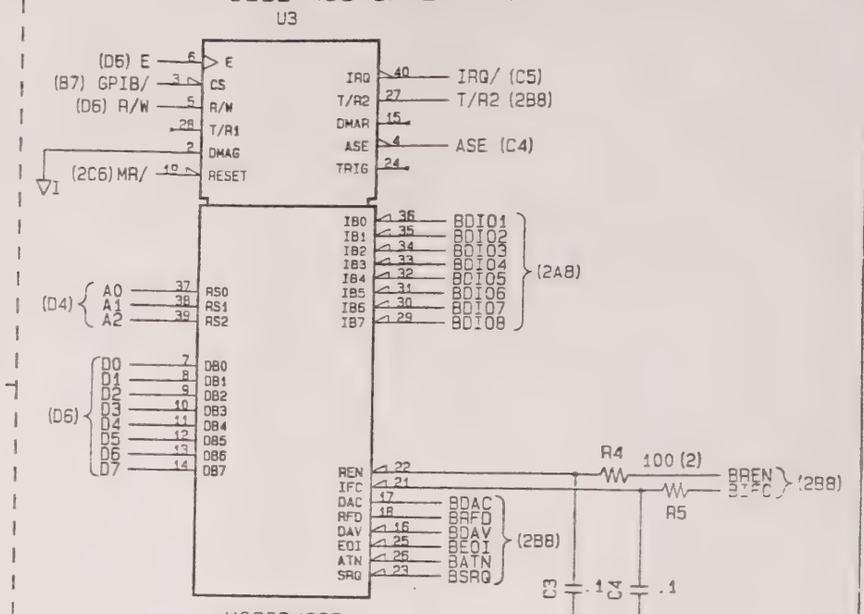
ADDRESS LATCH



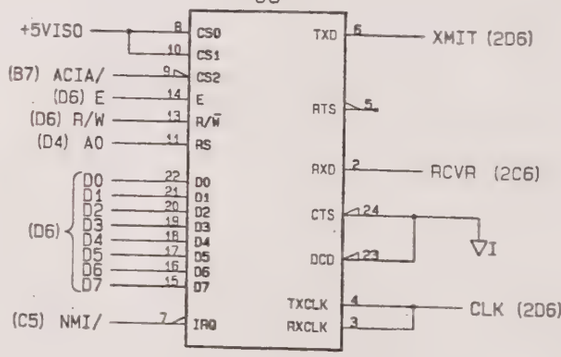
ADDRESS SWITCH / READ BUFFER



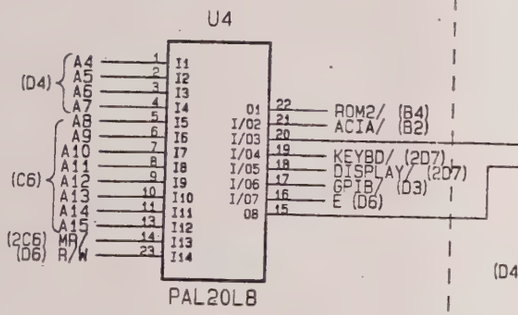
IEEE-488 INTERFACE



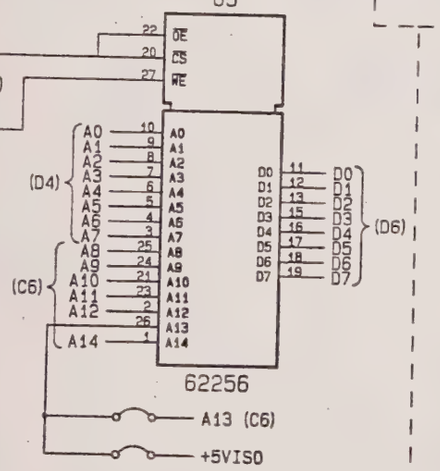
NOT USED



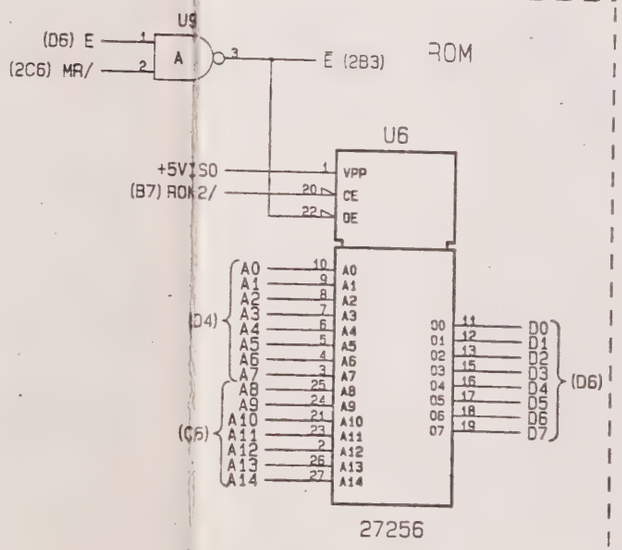
ADDRESS DECODER



RAM



ROM



2. ALL RESISTORS ARE IN OHMS , 1%, 1/8W, MF
1. ALL CAPACITORS ARE IN MICROFARADS

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. BUCKELL	DATE 3/14/89	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJECT ENG Ed Rosa	4/6/89	TITLE SCHEMATIC I/O PROCESSOR
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1° XX ± .030		
	DO NOT SCALE DWG		MODEL NO 680
	SCALE		DWG NO 1104-00-3236 REV B
			CODE IDENT 23338 SHEET 1 OF 2

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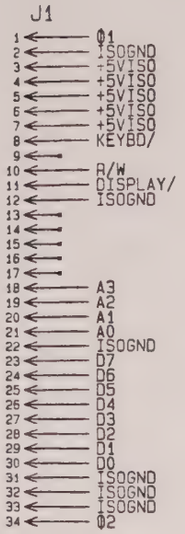
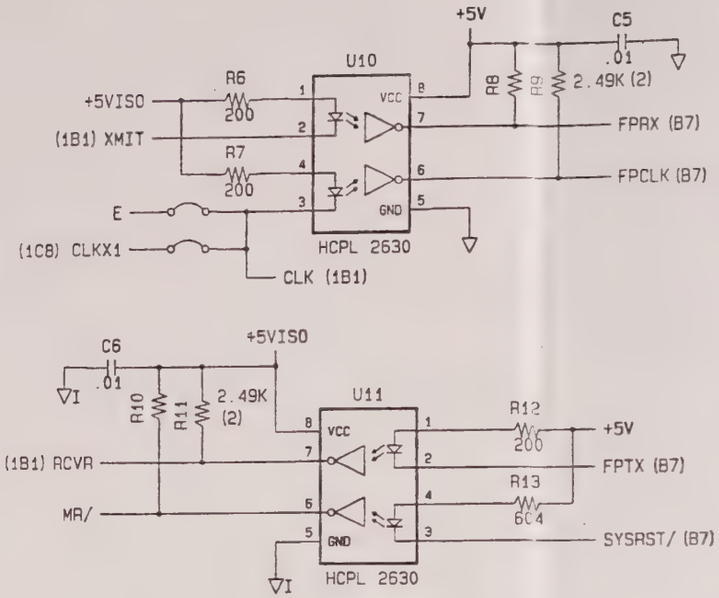
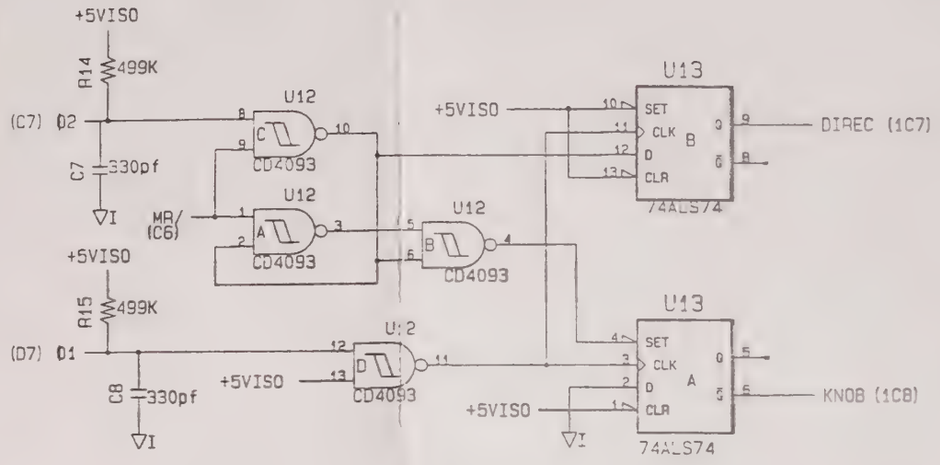


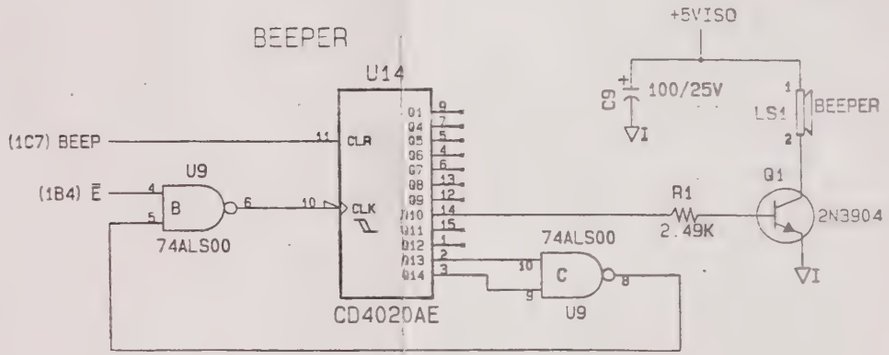
FRONT PANEL INTERFACE

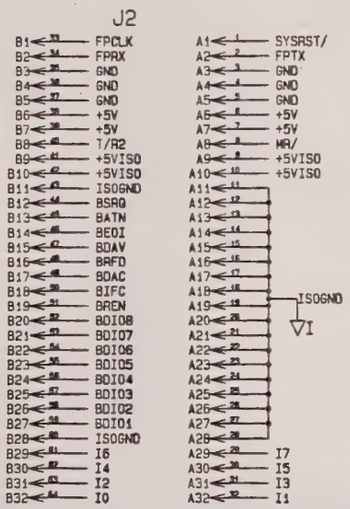


ISOLATED SERIAL INTERFACE

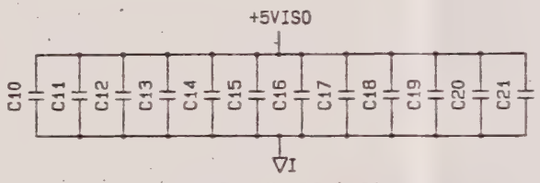


DIAL ENCOCER INTERFACE





MAIN INTERCONNECT BOARD CONNECTOR



.1 BY-PASS (12)

REF DES	U1	U2	U3	U4	U5	U6	U7	U8	U9	U12	U13	U14
+5VISO	7, 21	20	20	24	28	28	20	12	14	14	14	16
ISOGND	1	10	1	12	14	14	10	1	7	7	7	8
COMPONENT	6803	74ALS573	68488	20L8	6264	27256	74LS245	6850	74ALS00	4093	74ALS74	4020

REF DES LAST USED
U14 Y1 Q1
R15 J2
C21 RN2
CR1 LS1

NOTE: UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN D. Buzzell 3/24/83
PROJ ENGR C. Reuss 4/83
RELEASED APPROVED
TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE
SCHEMATIC I/O PROCESSOR

MODEL NO 680
DWG NO 1104-00-3236
REV B
CODE IDENT 23338
SHEET 2 OF 2

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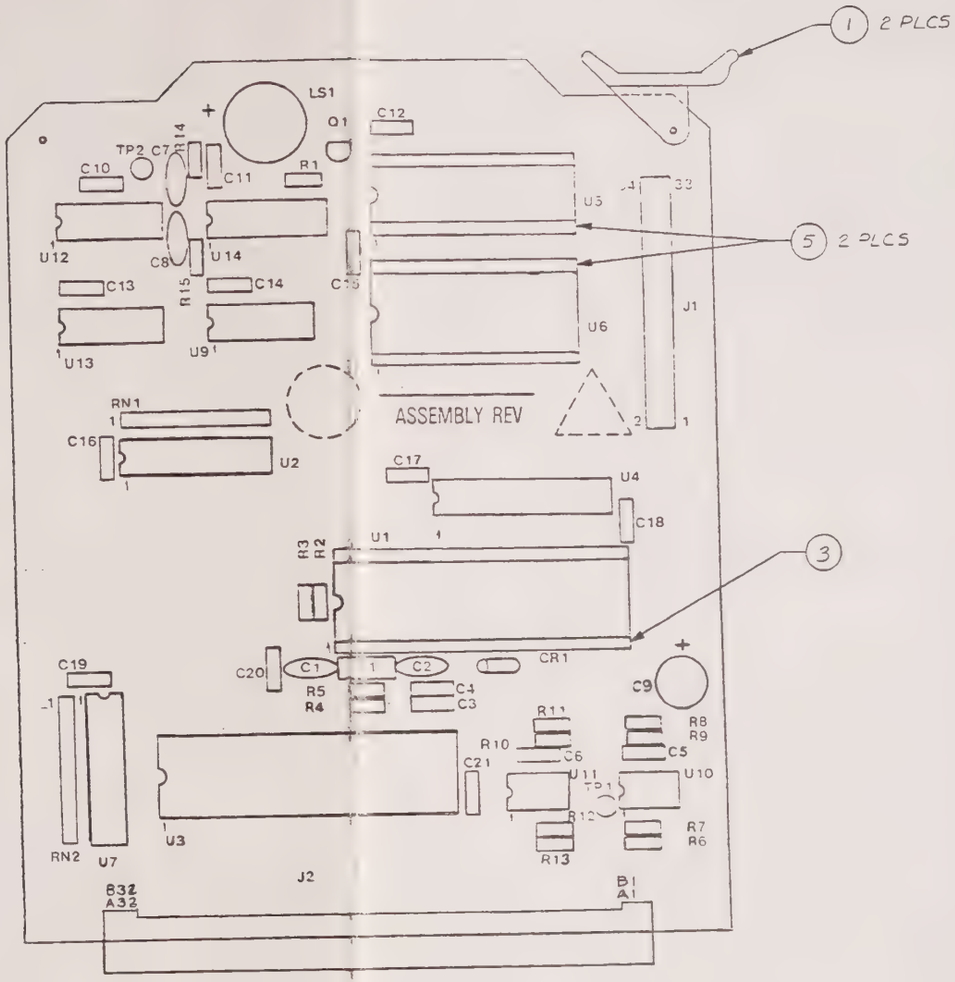
REV	ECN	BY	DATE	APP
A	ECO# 89-211	DB	3/24/89	



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. BUZZELL	DATE 3/24/89	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR Ed Rowe	4/88	TITLE INTERFACE PROCESSOR ASSEMBLY
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX : 010 ANGLES : 1 XX : 030		
	DO NOT SCALE DWG		MODEL NO 680 / DWG NO 1101-00-3236 / REV A
	SCALE 2/1		CODE IDENT 23338 / SHEET 1 OF 1

BISHOP GRAPHICS / ACCUPRESS

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REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
NONE	A/D-I/O PROCESSOR BD	1101-00-3236	WVTK	1101-00-3236	1
NONE	SCHEMATIC, I/O PROCESSOR BD	1104-00-3236	WVTK	1104-00-3236	1
C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C3 C4 C5 C6	CAP CER MON .1MF 50V Z5U +80/-20% RAD LD SP .2 BP .2	SR215E104ZAA	AVX	1500-01-0420	16
C1 C2	CAP, MICA, 27PF, 500V	DM15-270J	ARCO	1500-12-7000	2
C7 C8	CAP, MICA, 330PF, 500V	DM15-331J	ARCO	1500-13-3100	2
C9	CAP, ELECT, 100MF, 35V RADIAL LEAD, SP 20	NRE101M35V10X12.5(DB6)	NIC	1500-31-0102	1
NONE	DRILL DRWG, I/O PROCESSOR BOARD REF: SPEC 0006-00-0455 REV E	1700-00-2813	WVTK	1700-00-2813	1
J2	CONN, DIN, M PCMT, 64 PIN	PI64B20P00F00I1	BURND	2100-02-0158	1
3	SKT, IC, 40PIN	DILB40P-108T	BURND	2100-03-0030	1
5	SKT, IC, 28PIN	DILB28P-108T	BURND	2100-03-0055	2
TP1 TP2	TEST POINT, PC-TYPE	2100-04-0055	WVTK	2100-05-0024	2
J1	CONN, HEADER, 34 PIN	929836-01-17	AP	2100-05-0041	1
Y1	CRYSTAL, 8MHZ, SER, HC49	FOX080	FOX	2300-99-0030	1

WAVETEK PARTS LIST | TITLE PCA, I/O PROCESSOR BD | ASSEMBLY NO. 1100-00-3236 | REV D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	/HC18				
1	PC BD EJECTOR	103 WHITE	CALMK	2800-07-0008	2
LS1	BEEPER	GMB-06	STMIC	3000-00-0085	1
R4 R5	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	2
R12 R13 R6 R7	RES, MF, 1/8W, 1%, 200	RN55D-2000F	TRW	4701-03-2000	4
R2 R3	RES, MF, 1/8W, 1%, 2.21K	RN55D-2211F	TRW	4701-03-2211	2
R1 R10 R11 R8 R9	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	5
R14 R15	RES, MF, 1/8W, 1%, 499K	RN55D-4993F	TRW	4701-03-4993	2
RN2	RES NETWORK 10K 2% 10PIN SIP BUSS	4310R-101-103	BOURN	4770-00-0008	1
RN1	RES NETWORK 2.2K 2% 10PIN SIP BUSS	4310R-101-222	BOURN	4770-00-0011	1
CR1	DIODE 5082-2811 SCHOTTKY, 15V, 20MA	5082-2811	HP	4809-02-2811	1
Q1	TRANS 2N3904 NPN GENERAL PURPOSE TO-92	2N3904	FAIR	4901-03-9040	1
U10 U11	OPTOCOUPL, DUAL, TTL	HCPL-2630	HP	8000-26-3000	2
U12	GATE, NAND, 8/TRG DUA, CMOS	CD4093BE	RCA	8000-40-9300	1

WAVETEK PARTS LIST | TITLE PCA, I/O PROCESSOR BD | ASSEMBLY NO. 1100-00-3236 | REV D

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U5	BRAM, 8KX8, 120NS, CMOS	CXK5864BP-12L	SONY	8000-62-6400	1
U1	MICROPROCESSOR, 8BIT, 2 MHZ	MC68B03P	MOT	8000-68-0310	1
U9	GATE, NAND, QUAD 2-INP, TTL	SN74LS00N	TI	8000-74-0010	1
U13	FLIP-FLOP, DUAL D, POS EDGE TRIG W/CLR/PRES	SN74ALS74N	TI	8000-74-7403	1
U14	COUNTER, BIN, RIP/CAR, 6 MOS	CD4020BE	RCA	8001-40-2000	1
U3	ADPT, GPIB INTERFACE, 2.0 MHZ	MC68B488P	MOT	8006-84-8810	1
U7	XCVR, OCT BUS, TTL	74LS245	TI	8007-42-4510	1
U2	LATCH, OCTAL D	SN74ALS573CN	TI	8007-45-7310	1
U4	PAL, PROG, USES 1 EA 8000-20-8000 FOR MODEL 680 VER 1.0	8600-00-0455	WVTK	8600-00-0455	1
U6	PROG, EPROM, USES 8002-72-3600 FOR MOD 680MATE, REF U6, V5.2	8600-00-0675	WVTK	8600-00-0675	1

WAVETEK PARTS LIST | TITLE PCA, I/O PROCESSOR BD | ASSEMBLY NO. 1100-00-3236 | REV D

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: PARTS LIST I/O PROCESSOR BOARD
	PROJ. ENGR.		
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± XX = .XXX = ±		SIZE D | PROM NO. 23338 | DWG. NO. 1100-00-3236 | REV D; SCALE | MODEL 869 | SHEET 1 OF 1

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REV	ECN	BY	DATE	APP
A	ECO #89-669	MS	7/10/89	
B	ECO #90-390	MA	8.15.90	

R8 49.9 Ω: -2V — STRIG
R5 49.9 Ω: -2V — SSYNC

SUM BUS CLAMP

+5V
R1 4.99K
CR4 CR5 CR6 CR7 CR3 CR8
FD777 (6)
ANASUM
R3 51.1 Ω
R2 4.99K
-5V

ECL & CLOCK BUS TERMINATION

-2V
C11 1 TANT
RN20 50: 10MHZ, 10MHZ/, ECL1, ECL0, ECL2, ECL3
RN21 50: ECL4, ECL6, ECL5, ECL7, 100MHZ/, 100MHZ

TTL BUS TERMINATION

+3V
C24 .1, C26 .1
RN30: TTL0, TTL1
RN31: TTL2, TTL4, TTL6, TTL8, TTL10, TTL12, TTL14, TTL16, TTL18
RN32: TTL3, TTL5, TTL7, TTL9, TTL11, TTL13, TTL15, TTL17, TTL19
330 (3)

VME BUS TERMINATION

+3V
C14 .1
RN36: D31, D30, D29, D28, D27, D26, D25, D24
RN1: A8, A9, A10, A11, A12, A13, A14, A15, A16
RN4: IRQ1/, IRQ2/, IRQ3/, IRQ4/, IRQ5/, IRQ6/, IRQ7/, SERDAT, SERCLK
RN7: A1, A2, A3, A4, A5, A6, A7, AM4, A17
470 (12)
+3V
C20 .1
RN37: D23, D22, D21, D20, D19, D18, D17, D16
RN2: A18, AM3, A20, AS/, A22, BR3/, AM5, BR1/, SYSRST/
RN5: A19, AM2, A21, AM0, A23, BR2/, LWORD/, BR0/, BERR/
RN8: IACK/, AM1, DTACK/, WRITE/, DS0/, DS1/
+3V
C25 .1
RN38: A31, A30, A29, A28, A27, A26, A25, A24
RN3: SYSFAIL/, D15, D13, ACFAIL/, D9, BBSY/
RN6: D14, D6, D12, D4, D2, BCLR/, D0
RN9: SYSCLK, D7, D5, D11, D3, D10, D1, D8

3. SEE SHT. 4 of 4.
2. ALL RESISTORS IN OHMS
1. ALL CAPACITORS IN MICROFARADS

NOTE: UNLESS OTHERWISE SPECIFIED

MODULE #8

J3: C32 +24V, C31 DAC14, C30 REFCOM, C29 DCV8, C28 GND, C27 FRQ8, C26 GND, C25 FRQ0, C24 GND, C23, C22 GND, C21, C20 GND, C19, C18 GND, C17 SIG4, C16 GND, C15 SIG5, C14 GND, C13 SIG6, C12 GND, C11 GND, C10 ANASUM, C9 GND, C8 +10VR, C7 GND, C6 -5V, C5 -2V, C4 +5V, C3 -5V, C2 -5V, C1 -24V
J2: C32 +15V, C31 +15V, C30 GND, C29 +5V (MID1), C28 +5V (MID2), C27 +5V (MID0), C26 -5V, C25 ECL1, C24 -2V, C23 ECL3, C22 GND, C21 ECL5, C20 -2V, C19 ECL7, C18 -5V, C17 TTL1, C16 TTL3, C15 GND, C14 TTL5, C13 TTL7, C12 +5V(MID3), C11 TTL9, C10 TTL11, C9 GND, C8 TTL13, C7 TTL15, C6 +5V, C5 TTL17, C4 TTL19, C3 GND, C2 -15V, C1 -15V
J1: C32 +15V, C31 +15V, C30 GND, C29 +5V (MID1), C28 +5V (MID2), C27 +5V (MID0), C26 -5V, C25 ECL1, C24 -2V, C23 ECL3, C22 GND, C21 ECL5, C20 -2V, C19 ECL7, C18 -5V, C17 TTL1, C16 TTL3, C15 GND, C14 TTL5, C13 TTL7, C12 +5V(MID3), C11 TTL9, C10 TTL11, C9 GND, C8 TTL13, C7 TTL15, C6 +5V, C5 TTL17, C4 TTL19, C3 GND, C2 -15V, C1 -15V
J4: C32 +5V, C31 +12V, C30 A8, C29 A9, C28 A10, C27 A11, C26 A12, C25 A13, C24 A14, C23 A15, C22 A16, C21 A17, C20 A18, C19 A19, C18 A20, C17 A21, C16 A22, C15 A23, C14 AM5, C13 LWORD/, C12 SYSRST/, C11 BERR/, C10 SYSFAIL/, C9 GND, C8 D15, C7 D14, C6 D13, C5 D12, C4 D11, C3 D10, C2 D9, C1 D8
J5: B32 +5V, B31 +5VSTDBY, B30 IRQ1/, B29 IRQ2/, B28 IRQ3/, B27 IRQ4/, B26 IRQ5/, B25 IRQ6/, B24 IRQ7/, B23 GND, B22 SERDAT, B21 SERCLK, B20 GND, B19 AM3, B18 AM2, B17 AM1, B16 AM0, B15 BR3/, B14 BR2/, B13 BR1/, B12 BR0/, B11 BG3H/, B10 BG3L/, B9 BG2H/, B8 BG2L/, B7 BG1H/, B6 BG1L/, B5 BG0H/, B4 BG0L/, B3 ACFAIL/, B2 BCLR/, B1 BBSY/
J6: C32 +24V, C31 DAC12, C30 REFCOM, C29 DCV7, C28 GND, C27 FRQ7, C26 GND, C25 FRQ0, C24 GND, C23 SIG1F, C22 GND, C21 SIG2F, C20 GND, C19 SIG3F, C18 GND, C17 SIG4, C16 GND, C15 SIG5, C14 GND, C13 SIG6, C12 GND, C11 GND, C10 ANASUM, C9 GND, C8 +10VR, C7 GND, C6 -5V, C5 -2V, C4 +5V, C3 -5V, C2 -5V, C1 -24V
J7: A32 +24V, A31 DAC11, A30 TEMP, A29 DCV6, A28 GND, A27 FRQ6, A26 GND, A25 FRQ0, A24 GND, A23 SIG1E, A22 GND, A21 SIG2E, A20 GND, A19 SIG3E, A18 GND, A17 SIG4, A16 GND, A15 SIG5, A14 GND, A13 SIG6, A12 GND, A11 GND, A10 ANASUM, A9 GND, A8 -10VR, A7 GND, A6 -5V, A5 GND, A4 +5V, A3 -2V, A2 -5V, A1 -24V
J8: C32 +15V, C31 +15V, C30 GND, C29 +5V (MID0), C28 GND (MID1), C27 +5V (MID2), C26 -5V, C25 ECL1, C24 -2V, C23 ECL3, C22 GND, C21 ECL5, C20 -2V, C19 ECL7, C18 -5V, C17 TTL1, C16 TTL3, C15 GND, C14 TTL5, C13 TTL7, C12 +5V(MID3), C11 TTL9, C10 TTL11, C9 GND, C8 TTL13, C7 TTL15, C6 +5V, C5 TTL17, C4 TTL19, C3 GND, C2 -15V, C1 -15V
B32 +5V, B31 GND, B30 D31, B29 D30, B28 D29, B27 D28, B26 D27, B25 D26, B24 D25, B23 D24, B22 GND, B21 D23, B20 D22, B19 D21, B18 D20, B17 D19, B16 D18, B15 D17, B14 D16, B13 +5V, B12 GND, B11 A31, B10 A30, B9 A29, B8 A28, B7 A27, B6 A26, B5 A25, B4 A24, B3, B2 GND, B1 +5V
A32 10MHZ, A31 10MHZ/, A30 -2V, A29 STRIG, A28 STRIG, A27 GND, A26 SSYNC, A25 SSYNC, A24 -2V, A23 ECL0, A22 ECL2, A21 GND, A20 ECL4, A19 ECL6, A18 -5V, A17 TTL0, A16 TTL2, A15 GND, A14 TTL4, A13 TTL6, A12 +5V, A11 TTL8, A10 TTL10, A9 GND, A8 TTL12, A7 TTL14, A6 GND, A5 TTL16, A4 TTL18, A3 GND, A2 100MHZ/, A1 100MHZ

MODULE #7

J6: C32 +24V, C31 DAC12, C30 REFCOM, C29 DCV7, C28 GND, C27 FRQ7, C26 GND, C25 FRQ0, C24 GND, C23 SIG1F, C22 GND, C21 SIG2F, C20 GND, C19 SIG3F, C18 GND, C17 SIG4, C16 GND, C15 SIG5, C14 GND, C13 SIG6, C12 GND, C11 GND, C10 ANASUM, C9 GND, C8 +10VR, C7 GND, C6 -5V, C5 -2V, C4 +5V, C3 -5V, C2 -5V, C1 -24V
J9: A32 +24V, A31 DAC13, A30 TEMP, A29 DCV7, A28 GND, A27 FRQ7, A26 GND, A25 FRQ0, A24 GND, A23 SIG1F, A22 GND, A21 SIG2F, A20 GND, A19 SIG3F, A18 GND, A17 SIG4, A16 GND, A15 SIG5, A14 GND, A13 SIG6, A12 GND, A11 GND, A10 ANASUM, A9 GND, A8 -10VR, A7 GND, A6 -5V, A5 GND, A4 +5V, A3 -2V, A2 -5V, A1 -24V
J5: C32 +15V, C31 +15V, C30 GND, C29 GND (MID0), C28 +5V (MID1), C27 +5V (MID2), C26 -5V, C25 ECL1, C24 -2V, C23 ECL3, C22 GND, C21 ECL5, C20 -2V, C19 ECL7, C18 -5V, C17 TTL1, C16 TTL3, C15 GND, C14 TTL5, C13 TTL7, C12 +5V (MID3), C11 TTL9, C10 TTL11, C9 GND, C8 TTL13, C7 TTL15, C6 +5V, C5 TTL17, C4 TTL19, C3 GND, C2 -15V, C1 -15V
B32 +5V, B31 GND, B30 D31, B29 D30, B28 D29, B27 D28, B26 D27, B25 D26, B24 D25, B23 D24, B22 GND, B21 D23, B20 D22, B19 D21, B18 D20, B17 D19, B16 D18, B15 D17, B14 D16, B13 +5V, B12 GND, B11 A31, B10 A30, B9 A29, B8 A28, B7 A27, B6 A26, B5 A25, B4 A24, B3, B2 GND, B1 +5V
A32 10MHZ, A31 10MHZ/, A30 -2V, A29 STRIG, A28 STRIG, A27 GND, A26 SSYNC, A25 SSYNC, A24 -2V, A23 ECL0, A22 ECL2, A21 GND, A20 ECL4, A19 ECL6, A18 -5V, A17 TTL0, A16 TTL2, A15 GND, A14 TTL4, A13 TTL6, A12 +5V, A11 TTL8, A10 TTL10, A9 GND, A8 TTL12, A7 TTL14, A6 GND, A5 TTL16, A4 TTL18, A3 GND, A2 100MHZ/, A1 100MHZ
J4: C32 +5V, C31 +12V, C30 A8, C29 A9, C28 A10, C27 A11, C26 A12, C25 A13, C24 A14, C23 A15, C22 A16, C21 A17, C20 A18, C19 A19, C18 A20, C17 A21, C16 A22, C15 A23, C14 AM5, C13 LWORD/, C12 SYSRST/, C11 BERR/, C10 SYSFAIL/, C9 GND, C8 D15, C7 D14, C6 D13, C5 D12, C4 D11, C3 D10, C2 D9, C1 D8
J7: B32 +5V, B31 +5VSTDBY, B30 IRQ1/, B29 IRQ2/, B28 IRQ3/, B27 IRQ4/, B26 IRQ5/, B25 IRQ6/, B24 IRQ7/, B23 GND, B22 SERDAT, B21 SERCLK, B20 GND, B19 AM3, B18 AM2, B17 AM1, B16 AM0, B15 BR3/, B14 BR2/, B13 BR1/, B12 BR0/, B11 BG3H/, B10 BG3L/, B9 BG2H/, B8 BG2L/, B7 BG1H/, B6 BG1L/, B5 BG0H/, B4 BG0L/, B3 ACFAIL/, B2 BCLR/, B1 BBSY/
A32 +5V, A31 -12V, A30 A1, A29 A2, A28 A3, A27 A4, A26 A5, A25 A6, A24 A7, A23 AM4, A22 IACKB/, A21 IACK7/, A20 IACK/, A19 GND, A18 AM3, A17 AM2, A16 AM1, A15 AM0, A14 WRITE/, A13 DS0/, A12 DS1/, A11 GND, A10 SYSCLK, A9 GND, A8 D7, A7 D6, A6 D5, A5 D4, A4 D3, A3 D2, A2 D1, A1 D0

BATTERY BACK UP

+5VSTDBY
BR1/2A (2)
BT1, BT2

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN M.SMITH / RO FIFER	DATE 7/10/89	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC MAIN INTERCONNECT
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX : 010 ANGLES : 1° XX : 030		
	DO NOT SCALE DWG		
	SCALE		MODEL NO 680 · DWG NO. 1104-00-3295 · REV B
			CODE IDENT 23338 · SHEET 1 OF 4

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REV	ECN	BY	DATE	APP

MODULE #5

J12

C32	+24V	B32	+5V	A32	+24V
C31	DAC8	B31	GND	A31	DAC9
C30	REFCOM	B30	D31	A30	TEMP
C29	DCV5	B29	D30	A29	DCV5
C28	GND	B28	D29	A28	GND
C27	FRQ5	B27	D28	A27	FRQ5
C26	GND	B26	D27	A26	GND
C25	FRQ0	B25	D26	A25	FRQ0
C24	GND	B24	D25	A24	GND
C23	SI61E	B23	D24	A23	SI61D
C22	GND	B22	GND	A22	GND
C21	SI62E	B21	D23	A21	SI62D
C20	GND	B20	D22	A20	GND
C19	SI63E	B19	D21	A19	SI63D
C18	GND	B18	D20	A18	GND
C17	SI64	B17	D19	A17	SI64
C16	GND	B16	D18	A16	GND
C15	SI65	B15	D17	A15	SI65
C14	GND	B14	D16	A14	GND
C13	SI66	B13	+5V	A13	SI66
C12	GND	B12	GND	A12	GND
C11	GND	B11	A31	A11	GND
C10	ANASUM	B10	A30	A10	ANASUM
C9	GND	B9	A29	A9	GND
C8	+10VR	B8	A28	A8	-10VR
C7	GND	B7	A27	A7	GND
C6	-5V	B6	A26	A6	-5V
C5	-2V	B5	A25	A5	GND
C4	+5V	B4	A24	A4	+5V
C3	-5V	B3		A3	-2V
C2	-5V	B2	GND	A2	-5V
C1	-24V	B1	+5V	A1	-24V

J11

C32	+15V	B32	+5V	A32	10MHZ
C31	+15V	B31	GND	A31	10MHZ/
C30	GND	B30	D31	A30	-2V
C29	GND (MID0)	B29	D30	A29	STRIG
C28	GND (MID1)	B28	D29	A28	STRIG
C27	+5V (MID2)	B27	D28	A27	GND
C26	-5V	B26	D27	A26	SSYNC
C25	ECL1	B25	D26	A25	SSYNC
C24	-2V	B24	D25	A24	-2V
C23	ECL3	B23	D24	A23	ECL0
C22	GND	B22	GND	A22	ECL2
C21	ECL5	B21	D23	A21	GND
C20	-2V	B20	D22	A20	ECL4
C19	ECL7	B19	D21	A19	ECL6
C18	-5V	B18	D20	A18	-5V
C17	TTL1	B17	D19	A17	TTL0
C16	TTL3	B16	D18	A16	TTL2
C15	GND	B15	D17	A15	GND
C14	TTL5	B14	D16	A14	TTL4
C13	TTL7	B13	+5V	A13	TTL6
C12	+5V (MID3)	B12	GND	A12	+5V
C11	TTL9	B11	A31	A11	TTL8
C10	TTL11	B10	A30	A10	TTL10
C9	GND	B9	A29	A9	GND
C8	TTL13	B8	A28	A8	TTL12
C7	TTL15	B7	A27	A7	TTL14
C6	+5V	B6	A26	A6	GND
C5	TTL17	B5	A25	A5	TTL16
C4	TTL19	B4	A24	A4	TTL18
C3	GND	B3		A3	GND
C2	-15V	B2	GND	A2	100MHZ/
C1	-15V	B1	+5V	A1	100MHZ

J10

C32	+5V	B32	+5V	A32	+5V
C31	+12V	B31	+5VSTDBY	A31	-12V
C30	A8	B30	IRQ1/	A30	A1
C29	A9	B29	IRQ2/	A29	A2
C28	A10	B28	IRQ3/	A28	A3
C27	A11	B27	IRQ4/	A27	A4
C26	A12	B26	IRQ5/	A26	A5
C25	A13	B25	IRQ6/	A25	A6
C24	A14	B24	IRQ7/	A24	A7
C23	A15	B23	GND	A23	AM4
C22	A16	B22	SERDAT	A22	IACK5/
C21	A17	B21	SERCLK	A21	IACK5/
C20	A18	B20	GND	A20	IACK/
C19	A19	B19	AM3	A19	GND
C18	A20	B18	AM2	A18	AS/
C17	A21	B17	AM1	A17	GND
C16	A22	B16	AM0	A16	DTACK/
C15	A23	B15	BR3/	A15	GND
C14	AM5	B14	BR2/	A14	WRITE/
C13	LWORD/	B13	BR1/	A13	DS0/
C12	SYSRST/	B12	BR0/	A12	DS1/
C11	BERR/	B11	B63F/	A11	GND
C10	SYSFAIL/	B10	B63E/	A10	SYSCLK
C9	GND	B9	B62F/	A9	GND
C8	D15	B8	B62E/	A8	D7
C7	D14	B7	B61F/	A7	D6
C6	D13	B6	B61E/	A6	D5
C5	D12	B5	B60F/	A5	D4
C4	D11	B4	B60E/	A4	D3
C3	D10	B3	ACFAIL/	A3	D2
C2	D9	B2	BCLR/	A2	D1
C1	D8	B1	BBSY/	A1	D0

NOTE: UNLESS OTHERWISE SPECIFIED

MODULE #4

J15

C32	+24V	B32	+5V	A32	+24V
C31	DAC6	B31	GND	A31	DAC7
C30	REFCOM	B30	D31	A30	TEMP
C29	DCV4	B29	D30	A29	DCV4
C28	GND	B28	D29	A28	GND
C27	FRQ4	B27	D28	A27	FRQ4
C26	GND	B26	D27	A26	GND
C25	FRQ0	B25	D26	A25	FRQ0
C24	GND	B24	D25	A24	GND
C23	SI61D	B23	D24	A23	SI61C
C22	GND	B22	GND	A22	GND
C21	SI62D	B21	D23	A21	SI62C
C20	GND	B20	D22	A20	GND
C19	SI63D	B19	D21	A19	SI63C
C18	GND	B18	D20	A18	GND
C17	SI64	B17	D19	A17	SI64
C16	GND	B16	D18	A16	GND
C15	SI65	B15	D17	A15	SI65
C14	GND	B14	D16	A14	GND
C13	SI66	B13	+5V	A13	SI66
C12	GND	B12	GND	A12	GND
C11	GND	B11	A31	A11	GND
C10	ANASUM	B10	A30	A10	ANASUM
C9	GND	B9	A29	A9	GND
C8	+10VR	B8	A28	A8	-10VR
C7	GND	B7	A27	A7	GND
C6	-5V	B6	A26	A6	-5V
C5	-2V	B5	A25	A5	GND
C4	+5V	B4	A24	A4	+5V
C3	-5V	B3		A3	-2V
C2	-5V	B2	GND	A2	-5V
C1	-24V	B1	+5V	A1	-24V

J14

C32	+15V	B32	+5V	A32	10MHZ
C31	+15V	B31	GND	A31	10MHZ/
C30	GND	B30	D31	A30	-2V
C29	+5V (MID0)	B29	D30	A29	STRIG
C28	+5V (MID1)	B28	D29	A28	STRIG
C27	GND (MID2)	B27	D28	A27	GND
C26	-5V	B26	D27	A26	SSYNC
C25	ECL1	B25	D26	A25	SSYNC
C24	-2V	B24	D25	A24	-2V
C23	ECL3	B23	D24	A23	ECL0
C22	GND	B22	GND	A22	ECL2
C21	ECL5	B21	D23	A21	GND
C20	-2V	B20	D22	A20	ECL4
C19	ECL7	B19	D21	A19	ECL6
C18	-5V	B18	D20	A18	-5V
C17	TTL1	B17	D19	A17	TTL0
C16	TTL3	B16	D18	A16	TTL2
C15	GND	B15	D17	A15	GND
C14	TTL5	B14	D16	A14	TTL4
C13	TTL7	B13	+5V	A13	TTL6
C12	+5V (MID3)	B12	GND	A12	+5V
C11	TTL9	B11	A31	A11	TTL8
C10	TTL11	B10	A30	A10	TTL10
C9	GND	B9	A29	A9	GND
C8	TTL13	B8	A28	A8	TTL12
C7	TTL15	B7	A27	A7	TTL14
C6	+5V	B6	A26	A6	GND
C5	TTL17	B5	A25	A5	TTL16
C4	TTL19	B4	A24	A4	TTL18
C3	GND	B3		A3	GND
C2	-15V	B2	GND	A2	100MHZ/
C1	-15V	B1	+5V	A1	100MHZ

J13

C32	+5V	B32	+5V	A32	+5V
C31	+12V	B31	+5VSTDBY	A31	-12V
C30	A8	B30	IRQ1/	A30	A1
C29	A9	B29	IRQ2/	A29	A2
C28	A10	B28	IRQ3/	A28	A3
C27	A11	B27	IRQ4/	A27	A4
C26	A12	B26	IRQ5/	A26	A5
C25	A13	B25	IRQ6/	A25	A6
C24	A14	B24	IRQ7/	A24	A7
C23	A15	B23	GND	A23	AM4
C22	A16	B22	SERDAT	A22	IACK5/
C21	A17	B21	SERCLK	A21	IACK4/
C20	A18	B20	GND	A20	IACK/
C19	A19	B19	AM3	A19	GND
C18	A20	B18	AM2	A18	AS/
C17	A21	B17	AM1	A17	GND
C16	A22	B16	AM0	A16	DTACK/
C15	A23	B15	BR3/	A15	GND
C14	AM5	B14	BR2/	A14	WRITE/
C13	LWORD/	B13	BR1/	A13	DS0/
C12	SYSRST/	B12	BR0/	A12	DS1/
C11	BERR/	B11	B63E/	A11	GND
C10	SYSFAIL/	B10	B63D/	A10	SYSCLK
C9	GND	B9	B62E/	A9	GND
C8	D15	B8	B62D/	A8	D7
C7	D14	B7	B61E/	A7	D6
C6	D13	B6	B61D/	A6	D5
C5	D12	B5	B60E/	A5	D4
C4	D11	B4	B60D/	A4	D3
C3	D10	B3	ACFAIL/	A3	D2
C2	D9	B2	BCLR/	A2	D1
C1	D8	B1	BBSY/	A1	D0

MODULE #3

J18

C32	+24V	B32	+5V	A32	+24V
C31	DAC4	B31	GND	A31	DAC5
C30	REFCOM	B30	D31	A30	TEMP
C29	DCV3	B29	D30	A29	DCV3
C28	GND	B28	D29	A28	GND
C27	FRQ3	B27	D28	A27	FRQ3
C26	GND	B26	D27	A26	GND
C25	FRQ0	B25	D26	A25	FRQ0
C24	GND	B24	D25	A24	GND
C23	SI61C	B23	D24	A23	SI61B
C22	GND	B22	GND	A22	GND
C21	SI62C	B21	D23	A21	SI62B
C20	GND	B20	D22	A20	GND
C19	SI63C	B19	D21	A19	SI63B
C18	GND	B18	D20	A18	GND
C17	SI64	B17	D19	A17	SI64
C16	GND	B16	D18	A16	GND
C15	SI65	B15	D17	A15	SI65
C14	GND	B14	D16	A14	GND
C13	SI66	B13	+5V	A13	SI66
C12	GND	B12	GND	A12	GND
C11	GND	B11	A31	A11	GND
C10	ANASUM	B10	A30	A10	ANASUM
C9	GND	B9	A29	A9	GND
C8	+10VR	B8	A28	A8	-10VR
C7	GND	B7	A27	A7	GND
C6	-5V	B6	A26	A6	-5V
C5	-2V	B5	A25	A5	GND
C4	+5V	B4	A24	A4	+5V
C3	-5V	B3		A3	-2V
C2	-5V	B2	GND	A2	-5V
C1	-24V	B1	+5V	A1	-24V

J17

C32	+15V	B32	+5V	A32	10MHZ
C31	+15V	B31	GND	A31	10MHZ/
C30	GND	B30	D31	A30	-2V
C29	GND (MID0)	B29	D30	A29	STRIG
C28	+5V (MID1)	B28	D29	A28	STRIG
C27	GND (MID2)	B27	D28	A27	GND
C26	-5V	B26	D27	A26	SSYNC
C25	ECL1	B25	D26	A25	SSYNC
C24	-2V	B24	D25	A24	-2V
C23	ECL3	B23	D24	A23	ECL0
C22	GND	B22	GND	A22	ECL2
C21	ECL5	B21	D23	A21	GND
C20	-2V	B20	D22	A20	ECL4
C19	ECL7	B19	D21	A19	ECL6
C18	-5V	B18	D20	A18	-5V
C17	TTL1	B17	D19	A17	TTL0
C16	TTL3	B16	D18	A16	TTL2
C15	GND	B15	D17	A15	GND
C14	TTL5	B14	D16	A14	TTL4
C13	TTL7	B13	+5V	A13	TTL6
C12	+5V (MID3)	B12	GND	A12	+5V
C11	TTL9	B11	A31	A11	TTL8
C10	TTL11	B10	A30	A10	TTL10
C9	GND	B9	A29	A9	GND
C8	TTL13	B8	A28	A8	TTL12
C7	TTL15	B7	A27	A7	TTL14
C6	+5V	B6	A26	A6	GND
C5	TTL17	B5	A25	A5	TTL16
C4	TTL19	B4	A24	A4	TTL18
C3	GND	B3		A3	GND
C2	-15V	B2	GND	A2	100MHZ/
C1	-15V	B1	+5V	A1	100MHZ

J16

C32	+5V	B32	+5V	A32	+5V
C31	+12V	B31	+5VSTDBY	A31	-12V
C30	A8	B30	IRQ1/	A30	A1
C29	A9	B29	IRQ2/	A29	A2
C28	A10	B28	IRQ3/	A28	A3
C27	A11	B27	IRQ4/	A27	A4
C26	A12	B26	IRQ5/	A26	A5
C25	A13	B25	IRQ6/	A25	A6
C24	A14	B24	IRQ7/	A24	A7
C23	A15	B23	GND	A23	AM4
C22	A16	B22	SERDAT	A22	IACK4/
C21	A17	B21	SERCLK	A21	IACK3/
C20	A18	B20	GND	A20	IACK/
C19	A19	B19	AM3	A19	GND
C18	A20	B18	AM2	A18	AS/
C17	A21	B17	AM1	A17	GND
C16	A22	B16	AM0	A16	DTACK/
C15	A23	B15	BR3/	A15	GND
C14	AM5	B14	BR2/	A14	WRITE/
C13	LWORD/	B13	BR1/	A13	DS0/
C12	SYSRST/	B12	BR0/	A12	DS1/
C11	BERR/	B11	B63D/	A11	GND
C10	SYSFAIL/	B10	B63C/	A10	SYSCLK
C9	GND	B9	B62D/	A9	GND
C8	D15	B8	B62C/	A8	D7
C7	D14	B7	B61D/	A7	D6
C6	D13	B6	B61C/	A6	D5
C5	D12	B5	B60D/	A5	D4
C4	D11	B4	B60C/	A4	D3
C3	D10	B3	ACFAIL/	A3	D2
C2	D9	B2	BCLR/	A2	D1
C1	D8	B1	BBSY/	A1	D0

MODULE #2

J21

C32	+24V	B32	+24V	A32	+24V
C31	DAC2	B31	DAC3	A31	DAC3
C30	REFCOM	B30	TEMP	A30	TEMP
C29	DCV2	B29	DCV2	A29	DCV2
C28	GND	B28	GND	A28	GND
C27	FRQ2	B27	FRQ2	A27	FRQ2
C26	GND	B26	GND	A26	GND
C25	FRQ0	B25	FRQ0	A25	FRQ0
C24	GND	B24	GND	A24	IMMI
C23	SI61B	B23	SI61A	A23	SI61A
C22	GND	B22	GND	A22	GND
C21	SI62B	B21	SI62A	A21	SI62A
C20	GND	B20	GND	A20	GND
C19	SI63B	B19	SI63A	A19	SI63A
C18	GND	B18	GND	A18	GND
C17	SI64	B17	SI64	A17	SI64
C16	GND	B16	GND	A16	GND
C15	SI65	B15	SI65	A15	SI65
C14	GND	B14	GND	A14	GND
C13	SI66	B13	SI66	A13	SI66
C12	GND	B12	GND	A12	GND
C11	GND	B11	GND	A11	GND
C10	ANASUM	B10	ANASUM	A10	ANASUM
C9	GND	B9	GND	A9	GND
C8	+10VR	B8	-10VR	A8	-10VR
C7	GND	B7	GND	A7	GND
C6	-5V	B6	-5V	A6	-5V
C5	-2V	B5	GND	A5	GND
C4	+5V	B4	+5V	A4	+5V
C3	-5V	B3	-2V	A3	-2V
C2	-5V	B2	-5V	A2	-5V
C1	-24V	B1	-24V	A1	-24V

J20

C32	+15V	B32	+5V	A32	10MHZ
C31	+15V	B31	GND	A31	10MHZ/
C30	GND	B30	D31	A30	-2V
C29	+5V (MID0)	B29	D30	A29	STRIG
C28	GND (MID1)	B28	D29	A28	STRIG
C27	GND (MID2)	B27	D28	A27	GND
C26	-5V	B26	D27	A26	SSYNC
C25	ECL1	B25	D26	A25	SSYNC
C24	-2V	B24	D25	A24	-2V
C23	ECL3	B23	D24	A23	ECL0
C22	GND	B22	GND	A22	ECL2
C21	ECL5	B21	D23	A21	GND
C20	-2V	B20	D22	A20	ECL4
C19	ECL7	B19	D21	A19	ECL6
C18	-5V	B18	D20	A18	-5V
C17	TTL1	B17	D19	A17	TTL0
C16	TTL3	B16	D18	A16	TTL2
C15	GND	B15	D17	A15	GND
C14	TTL5	B14	D16	A14	TTL4
C13	TTL7	B13	+5V	A13	TTL6
C12	+5V (MID3)	B12	GND	A12	+5V
C11	TTL9	B11	A31	A11	TTL8
C10	TTL11	B10	A30	A10	TTL10
C9	GND	B9	A29	A9	GND
C8	TTL13	B8	A28	A8	TTL12
C7	TTL15	B7	A27	A7	TTL14
C6	+5V	B6	A26	A6	GND
C5	TTL17	B5	A25	A5	TTL16
C4	TTL19	B4	A24	A4	TTL18
C3	GND	B3		A3	GND
C2	-15V	B2	GND	A2	100MHZ/
C1	-15V	B1	+5V	A1	100MHZ

J19

C32	+5V	B32	+5V	A32	+5V
C31	+12V	B31	+5VSTDBY	A31	-12V
C30	A8	B30	IRQ1/	A30	A1
C29	A9	B29	IRQ2/	A29	A2
C28	A10	B28	IRQ3/	A28	A3
C27	A11	B27	IRQ4/	A27	A4
C26	A12	B26	IRQ5/	A26	A5
C25	A13	B25	IRQ6/	A25	A6
C24	A14	B24	IRQ7/	A24	A7
C23	A15	B23	GND	A23	AM4
C22	A16	B22	SERDAT	A22	IACK3/
C21	A17	B21	SERCLK	A21	IACK2/
C20	A18	B20	GND	A20	IACK/
C19	A19	B19	AM3	A19	GND
C18	A20	B18	AM2	A18	AS/
C17	A21	B17	AM1	A17	GND
C16	A22	B16	AM0	A16	DTACK/
C15	A23	B15	BR3/	A15	GND
C14	AM5	B14	BR2/	A14	WRITE/
C13	LWORD/	B13	BR1/	A13	DS0/
C12	SYSRST/	B12	BR0/	A12	DS1/
C11	BERR/	B11	B63C/	A11	GND
C10	SYSFAIL/	B10	B63B/	A10	SYSCLK
C9	GND	B9	B62C/	A9	GND
C8	D15	B8	B62B/	A8	D7
C7	D14	B7	B61C/	A7	D6
C6	D13	B6	B61B/	A6	D5
C5	D12	B5	B60C/	A5	D4
C4	D11	B4	B60B/	A4	D3
C3	D10	B3	ACFAIL/	A3	D2
C2	D9	B2	BCLR/	A2	D1
C1	D8	B1	BBSY/	A1	D0

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN M. Smith / PD FIFER	DATE 10/	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC MAIN INTERCONNECT
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX : 010 ANGLES ±1° XX : 030		
	DO NOT SCALE DWG		MODEL NO 680 / DWG NO. 1104-00-3295 / REV B
	SCALE		CODE IDENT 23338 / SHEET 2 OF 4

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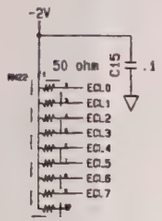
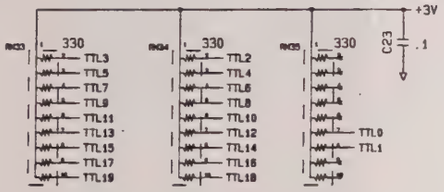
REV	ECN	BY	DATE	APP

TTL & ECL BUS TERMNIATION

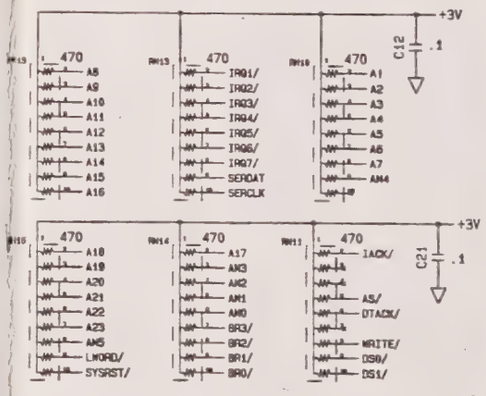




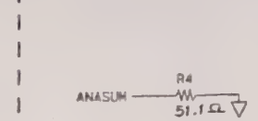
NOTE: UNLESS OTHERWISE SPECIFIED

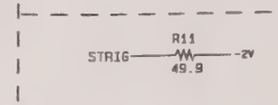
MODULE #1

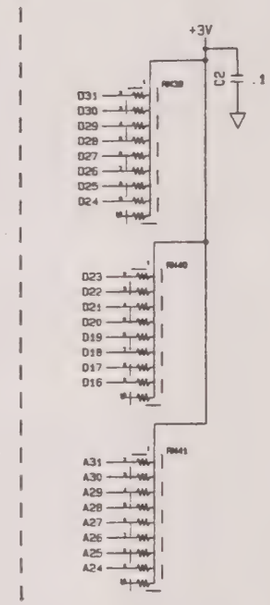
REF CAL



MICROPROCESSOR







P2 VME BUS TERMINATORS

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN M. SMITH / RO FIFER	DATE 10/4/89	WAVETEK SAN DIEGO, CALIFORNIA	
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC MAIN INTERCONNECT	
	RELEASE APPROV			
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX : ±.010 ANGLES : ±1° .XX : ±.030			
	DO NOT SCALE DWG		MODEL NO. 680	DWG NO. 1104-00-3295 REV B
	SCALE		CODE IDENT. 23338	SHEET 3 OF 4

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FRONT PANEL CONNECTOR

J30

B1	FPCLK	A1	SYSRST/1
B2	FPRX	A2	FPTX
B3	GND	A3	GND
B4	GND	A4	GND
B5	GND	A5	GND
B6	+5V	A6	+5V
B7	+5V	A7	+5V
B8	T/R2	A8	MR/
B9	+5VISO	A9	+5VISO
B10	+5VISO	A10	+5VISO
B11	ISOGND	A11	
B12	BSRQ	A12	
B13	BATN	A13	
B14	BEOI	A14	
B15	BDAV	A15	
B16	BAFD	A16	
B17	BDAC	A17	
B18	BIFC	A18	
B19	BREN	A19	
B20	BDIO8	A20	ISOGND
B21	BDIO7	A21	
B22	BDIO6	A22	
B23	BDIO5	A23	
B24	BDIO4	A24	
B25	BDIO3	A25	
B26	BDIO2	A26	
B27	BDIO1	A27	
B28	ISOGND	A28	
B29	I6	A29	I7
B30	I4	A30	I5
B31	I2	A31	I3
B32	I0	A32	I1

J34

1	+24V
2	GND
3	+5VISO
4	ISOGND
5	GND
6	GND
7	GND
8	GND

J33

1	-2V
2	-2V
3	GND
4	-5V
5	-5V
6	-5V
7	-5V
8	GND
9	-24V
10	+15V

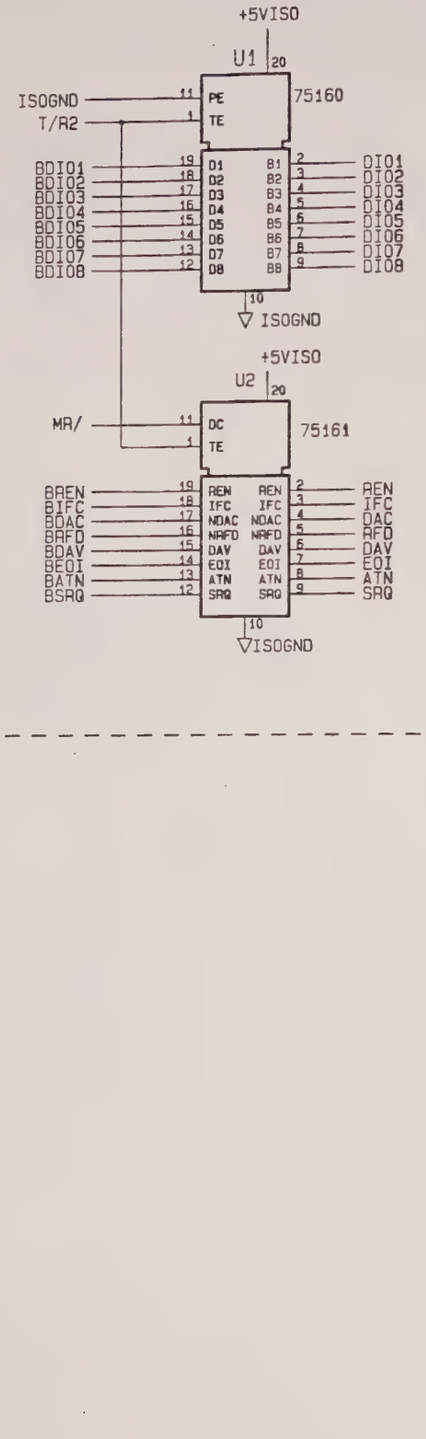
J32

1	GND
2	GND
3	GND
4	+5V
5	+5V
6	+5V
7	+5V
8	GND
9	-15V

POWER SUPPLY CONNECTOR

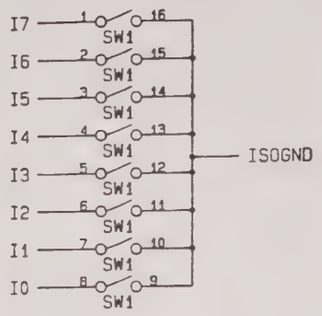
NOTE UNLESS OTHERWISE SPECIFIED

GPIB (IEEE-488) CONNECTOR

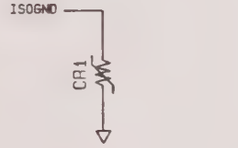


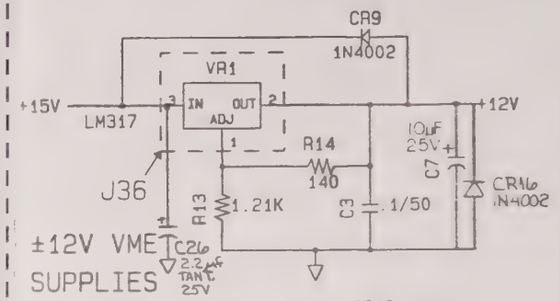
J31

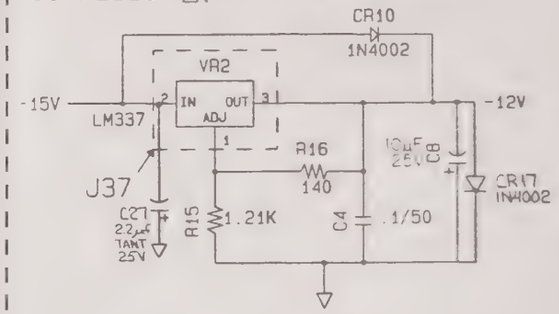
DIO1	1
DIO2	2
DIO3	3
DIO4	4
EOI	5
DAV	6
RFD	7
DAC	8
IFC	9
SRQ	10
ATN	11
CGND	12
DIO5	13
DIO6	14
DIO7	15
DIO8	16
REN	17
	18
	19
	20
	21
	22
	23
ISOGND	24

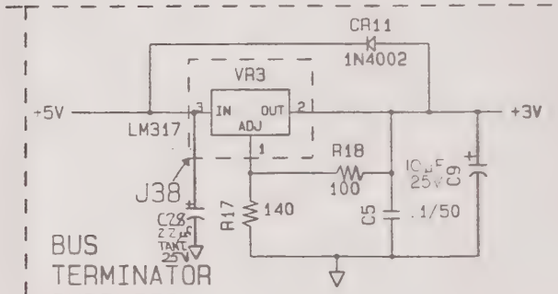


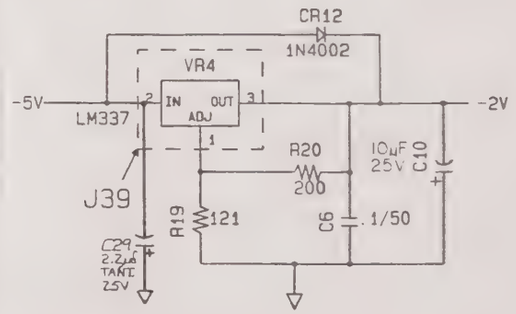
GPIB ADDRESS SELECTOR











REV	ECN	BY	DATE	APP

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN R. SMITH / PO FIFER	DATE 7/10/87	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC MAIN INTERCONNECT
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX: .010 ANGLES ±1° XX: .030		
	DO NOT SCALE DWG		MODEL NO. 680
	SCALE		DWG NO. 1104-00-3295 REV B
			CODE IDENT 23338 SHEET 4 OF 4

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REV	ECO	BY	DATE	APP
B	# 10-340 FOR RELEASE	JL	4/5/91	

INSTALL FARSIDE (2) (4)

(3 TYP) (10)

(11) SEE VIEW A (4 PLACES)

(12) APPROX 1.5"

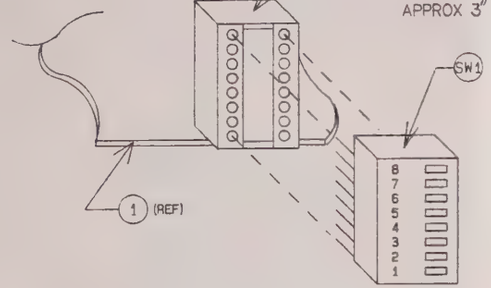
(12) APPROX 3"

(2)

(12) APPROX 3"

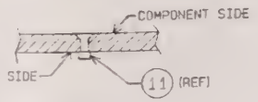
(1)

(2) (5)



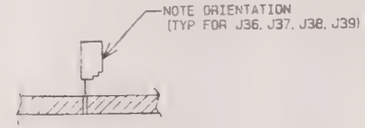
VIEW "B"

SW1 ADDRESS SWITCH INSTALLATION
(AS VIEWED FROM REAR OF BOARD)
SCALE: NONE



VIEW A

SWAGE STANDOFF
SCALE: NONE



VIEW C-C

3. ASSEMBLE PER WAVETEK WORKMANSHIP STANDARDS.
2. REFERENCE DESIGNATORS DO NOT APPEAR ON PARTS.
1. SEE 1104-00-3295 FOR SCHEMATIC.

NOTE UNLESS OTHERWISE SPECIFIED

CAD JOB #: B056A

SEE SEPARATE PARTS LIST 1100-00-3295

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE 3/5/91
MATERIAL	CHECKED	3/6/91
	PROJ. ENGR.	3/6/91
FINISH WAVETEK PROCESS	RELEASE APPROVAL	3/6/91
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ±.2 .XXX ±.1 ±	

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: PCA, MAIN INTERCONNECT

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1101-00-3295	B

SCALE .95 : 1 | MODEL 680 | SHEET 1 OF 2

1101-00-3295 B

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REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRAWING MAIN INTERCONNECT BOARD	1101-00-3295	WVTK	1101-00-3295	1
NONE	SCHEMATIC, MAIN INTERCONNECT BOARD	1104-00-3295	WVTK	1104-00-3295	1
C12 C14 C15 C2 C20 C21 C22 C23 C24 C25 C26 C3 C4 C5 C6	CAP CER MON .1MF 50V Z5U +80/-20% RAD LD SP .2 BP .2	SR215E104ZAA	AVX	1500-01-0420	15
C10 C11 C7 C8 C9	CAP, ELECT, 10MF/25V RADIAL LEAD, SP .10	NRE 10/63	NIC	1500-31-0002	5
C26 C27 C28 C29	CAP, TANT, 2.2MF, 25V	199D225X9025AA2	SPRAG	1500-72-2502	4
NONE	PCB ASSY, 680 MOTHER BD (4-4-91) REF SPEC 0008-00-0455 REV C	1700-00-3295	WVTK	1700-00-3295	1
J34	CONN, POWER	10-19-1081	MOLEX	2100-02-0239	1
J33	CONN, POWER	10-19-1101	MOLEX	2100-02-0240	1
J32	CONN, POWER	10-19-1091	MOLEX	2100-02-0241	1
J31	CONN, GPIB, REVERSE ORIENT W/CAP HARDWARE	553811-2	AMP	2100-02-0249	1
J12 J15 J18 J21 J24 J26 J3 J6 J9	CONN, DIN, RECP, PRESSFIT, F, 64PIN, 3-ROW, A&C	DIN-64-CSB-PS-TR	ROBNU	2100-02-0289	9
J1 J10 J11 J13 J14 J16 J17 J19 J2 J20 J22 J23 J25 J27	CONN, DIN, RECP, PREEFIT, F, 96 PIN	DIN-96-CSC-PS-TR	ROBNU	2100-02-0290	19

WAVETEK PARTS LIST | TITLE MAIN INTERCONNECT BOARD | ASSEMBLY NO. 1100-00-3295 | REV B | PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R1 R2	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	2
R11 R12 R5 R8	RES, MF, 1/8W, 1%, 49.9	RN55D-49R9F	CORNO	4701-03-4999	4
R3 R4	RES, MF, 1/8W, 1%, 51.1	RN55D-51R1F	TRW	4701-03-5119	2
RN1 RN10 RN11 RN12 RN13 RN14 RN15 RN16 RN17 RN18 RN2 RN3 RN36 RN37 RN38 RN39 RN4 RN40 RN41 RN5 RN6 RN7 RN8 RN9	RES NETWORK 470 10PIN SIP BUSS	4310R-101-471	BOURN	4770-00-0009	24
RN20 RN21 RN22	RES NETWORK, SINGLE 10 PIN, 50 OHM	4310R-101-500	BOURN	4770-00-0058	3
RN30 RN31 RN32 RN33 RN34 RN35	RES NETWORK, SINGLE 10 PIN, 330 OHM	4310R-101-331	BOURN	4770-00-0059	6
CR10 CR11 CR12 CR16 CR17 CR9	DIODE, 1N4002 GEN PURPOSE RECT, 100V, 1A	1N4002	FAIR	4801-02-0001	6
CR3 CR4 CR5 CR6 CR7 CR8	DIODE, ULTRA FAST	1N4244	T/CSF	4807-02-0777	6
CR1	DIODE, VARISTOR	V56ZA8	GE	4899-00-0043	1
SW1	SWITCH PC	2400080	EECO	5199-00-0004	1
12	TAPE	P-256-1/2"	PRMCL	5600-05-0010	8
U1	XCVR, OSC BUS, TTL	75160	TI	8007-51-6000	1
U2	TRANSCEIVER, OCT BUS,	SN75161BN	TI	8007-51-6100	1

WAVETEK PARTS LIST | TITLE MAIN INTERCONNECT BOARD | ASSEMBLY NO. 1100-00-3295 | REV B | PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
J28 J4 J5 J7 J8					
J30	CONN, DIN, RECP, PRESSFIT, F, 64 PIN, 2-ROW	21-6458-064-001-025	ELCO	2100-02-0291	1
J36 J37 J38 J39	SOCKET	10-18-2031	MOLEX	2100-03-0047	4
2	SKT, RT/A, 16 PIN	16-810-90	ARIES	2100-03-0079	1
10	SOCKET, CONTACT, SOLDER LESS, ZERO-PROFILE	322-HCS-5P3-300	AUGAT	2100-03-0109	370
11	STANDOFF, SWAGE, .125H, .140, .250 DIA, 6-32 THD	BR6910C-0.125-34	LYNTN	2800-06-0057	4
4	SCREW, 4X3/8 PHP SMS TYPE B RECESS, 4-40X3/8	4-24 X 3/8	CMRCL	2800-22-4162	2
5	BATTERY HOLDER	3000-00-0090	WVTK	3000-00-0090	2
BT1 BT2	BATTERY, LITHIUM, 3V	BR-1/2A	PANAS	4000-02-0007	2
R18	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	1
R19	RES, MF, 1/8W, 1%, 121	RN55D-1210F	TRW	4701-03-1210	1
R13 R15	RES, MF, 1/8W, 1%, 1.21K	RN55D-1211F	TRW	4701-03-1211	2
R14 R16 R17	RES, MF, 1/8W, 1%, 140	RN55D-1400F	TRW	4701-03-1400	3
R20	RES, MF, 1/8W, 1%, 200	RN55D-2000F	TRW	4701-03-2000	1

WAVETEK PARTS LIST | TITLE MAIN INTERCONNECT BOARD | ASSEMBLY NO. 1100-00-3295 | REV B | PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	TTL				

WAVETEK PARTS LIST | TITLE MAIN INTERCONNECT BOARD | ASSEMBLY NO. 1100-00-3295 | REV B | PAGE 4

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN | DATE | CHECKED | PROJ. ENGR. | RELEASE APPROV. | MATERIAL | FINISH WAVETEK PROCESS | DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± XX ± XXX ± ±

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: PARTS LIST MAIN INTERCONNECT BOARD

SIZE D | FSCM NO. 23338 | DWG. NO. 1100-00-3295 | REV B | SCALE | MODEL 869 | SHEET 1 OF 1

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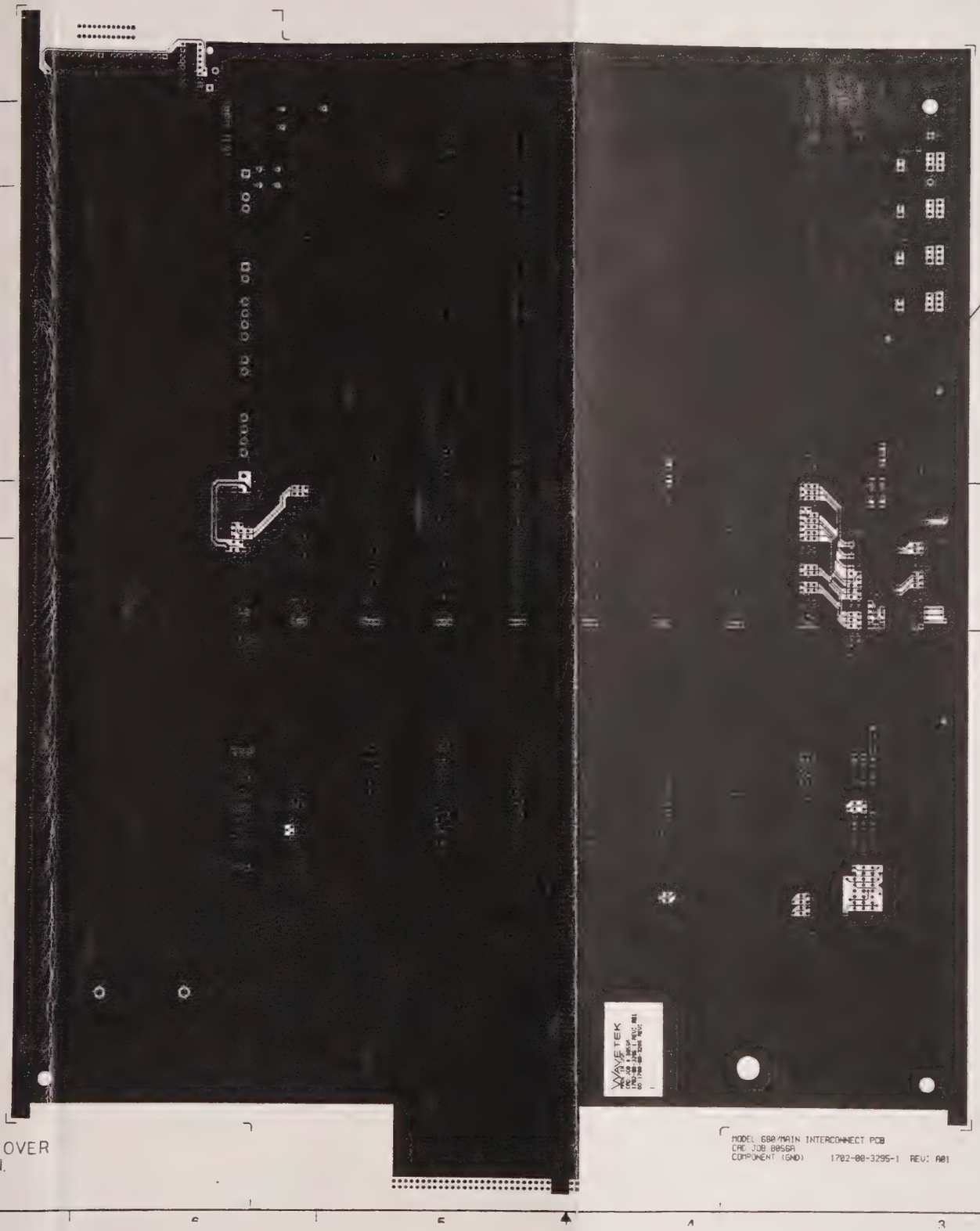
REV	ECO	BY	DATE	APP



MODEL 680/MAIN INTERCONNECT PCB
CAD JOB 8056A
COMPONENT (GND) 1702-00-3295-1 REV: A01

⚠ APPLY ITEM 12 (INSULATING TAPE) OVER TRACES IN 3 PLACES AS SHOWN.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE 4/19	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: PCA, MAIN INTERCONNECT
	PROJ. ENGR.		
FINISH WAVETEK PROCESS	RELEASE APPROV.		SIZE D · FSCM NO. 23338 · DWG. NO. 1101-00-3295 · REV B
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .XXX ±		SCALE · MODEL 680 · SHEET · OF

1101-00-3295 B

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REV	ECN	BY	DATE	APP
A	ECO# 90-213	MS	2/20/90	DB
B	ECO# 90-288	MS	3/30/90	DB
C	ECO# 91-398	KA	9/16/91	

MICROPROCESSOR

U5 6803

C6 27pf SM, C7 27pf SM, Y1 4MHz, TP2

CR17, CR1 HP2811 (2)

R2 10K, R3 10K

(4B2) STRADY, (BC8) SYSRST

(4D3) IOST1, (2C6) EXTREF, (2D5) REFSEL, (2A8, 2B3) SDIN

U6 74LS86 1/4 — E (B4, B5, C3, B4), BE (B8)

R/W (4B2, A6), AS (D5, 4B2, B4)

AD0–AD7 (D5, C5, A6, B6, 4C1, 4B2)

A8–A15 (A6, A8), (D3) R1 3.32K, IRQ (A6)

ADDRESS LATCH

U2 74ALS573 — (D6) A5, (D6) E, AD0–AD7, (D6), A0–A7 (B4, B5, B3, B3, B3, D4, B3, B5, B3, D3)

RN9 2.2K 2%

U3 74ALS573 — (D6) E, AD0–AD7, (D6), D0–D7 (5B3, 6C8, 7A7, A2, B2, C2)

RN1 2.2 K 2%

(2B8, 6C8, 7A7, A2, B2, C2)

DATA LATCH

ADDRESS DECODER

U8 74LS139 1/2 — (D4) A5, (D4) A6, CTR (4B2), REGS1 (B5), REGS2 (B4)

U58 74LS32 1/4 — A7 (D4)

U8 74LS139 1/2 — (C6) A14, (C6) A15, RAM (A6), ROM (B8)

U6 74LS86 1/4 — (BC8) SYSRST

CONTROL LATCHES

U11 74ALS574 — (B3) R6STB, (C4) D0–D7, CTRCH0–CTRCH5, TAGSLP, TAGMODE, (4B6), (4C4), (2B4)

U12 74ALS574 — (B3) R4STB, (C4) D0–D7, INTR0–INTR4, TRIG1–TRIG3, (5B3), (2D2)

U13 74ALS574 — (B3) R5STB, (C4) D0–D7, DVMCH0–DVMCH5, ITTRON, DVMRUN, (4D7), (5B4), (4C2), (4D4)

CONTROL DATA STROBE

U4 74LS138 — (D4) A0–A2, (D6) E, (D4) A7, (D3) REGS1, DACH1 (6D8), DACL0 (6C8), SH1 (6A8), SH2 (7A8), DNC2 (2B4), DNC1 (2B3)

U9 74LS138 — (D4) A0–A2, (D6) E, (D4) A7, (D3) REGS2, R0STB (2A7), R1STB (5B8), R2STB, R3STB (4C2), R4STB (C2), R5STB (B2), R6STB (D2)

U6 74LS86 1/4 — DNCE1 (2B3, 5B8)

E PROM MEMORY

U1 27128 — (D3) ROM, (D6) BE, +5V, (D4) A0–A7, (C6) A8–A13, (D6) D0–D7

68000 INTERFACE

U7 68HC34 — (BC8) SYSRST, +5V, (D6) E, (D6) AS, (D6) R/W, (D3) RAM, (C6) A8, IRQ, (D6) AD0–AD7, LE (8D8), +5V, CSRC (8C7), LA9 (8D7), AV2 (8C7), LA1–LA8 (8D8), LR/W (8C8)

U10 74LS245 — (A5, 8C7) CSRC, DIR (BA), DIR (AB), LD0–LD7 (8D8)

2. ALL CAPACITORS ARE IN MICROFARADS

1. ALL RESISTORS ARE IN OHMS, 1%, 1/8W, MF

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES — MATERIAL — FINISH WAVETEK PROCESS

DRAWN RO FIFER — DATE — PROJENGR — RELEASE APPROV

TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .020

DO NOT SCALE DWG — SCALE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: SCHEMATIC REF CAL

MODEL NO. 680 — DWG NO. 1104-00-3385 — REV C

CODE IDENT 23330 — SHEET 1 OF 8

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REV	ECN	BY	DATE	APP

TRIGGER SELECT

U23 74ALS151: (1B1) TRIG1, TRIG2, TRIG3; (B2) EXTTRIG; (B1) DLYTRIG; (5B2) INTTRIG; (5B3) INTTRG1; (B1) DIVTRIG; +5V; D0–D7; EN; A; B; C; Y; W

U60 1/4 10H124 (D); U60 1/4 10H124 (C); +5V; STRIG (8C8,3C7); TRIGMEAS (4B4)

U19 74LS74 1/2: (5B3) INTTRG1; +5V; SET, CLK, D, CLR, Q, Q̄

TRIGGER CONTROL

L1 390 nH; C22 10/25V ELEC; +5V

REF IN J100; R4 100; C23 470pf; R5 4.99K; R6 1K; R7 100; U15 NE521 (ST1, IN1A, IN1B, STS, IN2A, IN2B, ST2, OUT1, OUT2); REFCLK (4B4)

U14 CLK 10 MHZ TCXO; R8 499; 10MCLK (4B4)

R9 40.2K; R10 10K; C21 .1

R130 10K; REFSEL (1C7)

U16 74HC151: EN, A, B, C, D0–D7, Y, W

R11 1K; R12 1K; CR2 1N4148; EXTREF (1C7); Q1 2N3904; C18 .1

R13 750; HFCLK (5L8) (4B2)

U20 10H124 1/4: 10MHZ, 10MHZ (8C8); R23, R22 49.9 (2)

-2V

R14 499; Q2 2N3906 HP2811; CR3; C24 47pf; R16 825; R19 46.4; C19 .1; R17 1.21K; R20 46.4; C25 47pf; R18 825; CR4 HP2811; Q3 2N3904; R21 249; R15 499

REF OUT J101

TRIG IN J102; C30 2.7 pF; R24 12.4K; R25 3.01K; CR5 1N5282; CR6 1N5282; -5V

R45 150K; 74LS86 1/4 U6: (1C1) TRGSLP

U17 NE521: ST1, IN1A, IN1B, STS, IN2A, IN2B, ST2, OUT1, OUT2

R103 10.5K; +10VR (4A4); R28B 200; R28A 20K; R29 4.99K

U26 DAC0832: (1C4) D7–D1; (1C7) SDIN; D10–D17; RFB; VREF; IOUT1; IOUT2; CS; WR1; WR2; ILE; XFER; C44 .22; (4A6)+10VR; ROSTB (1B3); +15V

U27 TL082 1/2 (A); TL082 1/2 (B); R30 10K

C28 .01; C170 .1; R102 2K; DL1; R100 100; R101 100

(1C1) TRGMODE; (1B4) DNC2

U54 74LS157: A/B, EN, 1A–4A, 1B–4B, 1Y–4Y

U18 DNC2016: (8C8) SYSRST; (1B4) DNCK1; (1B4) DNCE1; (1C7) SDIN; +5V; MRES, SCLK, SEN, SDIN, PLD, TMEN; CLKA, SLDA, ALDA, CLKB, SLDB, ALDB, CYA, CYDA, CYB, CYOB

R132 10K; +5V

EXTTRIG (D3); DLYTRIG (D3); DIVTRIG (D3); 10MOSC (4B4)

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN A. SATTAR RO FIFER DATE 2-20-90	WAVETEK SAN DIEGO, CALIFORNIA	
MATERIAL	PROJ ENGR	TITLE	SCHEMATIC REF CAL
FINISH WAVETEK PROCESS	RELEASE APPROV	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030	
	DO NOT SCALE DWG	MODEL NO. 680	DWG NO. 1104-00-3385 REV C
	SCALE NONE	CODE IDENT 23338	SHEET 2 OF 8

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REV	ECO	BY	DATE	APP

+5V
R125 21.5
Q30 2N5771 (2) Q31
R142 21.5
R143 21.5
TRIGGER OUT
J103
R126 49.9 1% 1/2W
+5V +5V
R118 100
R33 100
R65 301
R64 301
CR16
CR15
HP2811 (2)
(2D1,8C8)STRIG
R140 46.4
Q28 2N3563 (2) Q29
R141 46.4
R121 82.5
C172 .1
CR19 CR18 HP2811 (2)
C171 .01
R119 332
-5V
R120 46.4
-2V

ANALOG SUM IN

SUMIN
J105
R117 100
R150 49.9 1% 1/2W
+15V
C173 .1
CR13 1N755 7.5V
R113 150
R110 316
Q32 2N2905A
Q26 2N3906
R116 2.49K
R124 51.1
ANASUM (8D5)
-15V
+15V
Q33 2N2219A
Q27 2N3904
R111 316
CR14 1N755 7.5V
R115 150
-15V
C174 .1

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DO NOT SCALE DRAWING
DRAWN
CHECKED
PROJ ENGR.
RELEASE APPROV
DATE
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES

WAVETEK SAN DIEGO, CALIFORNIA

TITLE
SCHEMATIC
REF CAL

SIZE D | FSCM NO. 23338 | DWG NO. 1104-00-3385 | REV C
SCALE | MODEL 680 | SHEET 3 OF 5

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REV	ECN	BY	DATE	APP

DVM AND GAIN SELECT

U34 DG508 — (1A1) DVMCH0, DVMCH1, DVMCH2 → A0, A1, A2; EN ← +5V; (8C5) DCV1–DCV8 → S1–S8; D → U52 pin 3

U52 LT1013 1/2 (A)

RN4: R1 5K, R2 5K, R3 5K, R4 5K; T914

U35 DG508 — (1A1) DVMCH3, DVMCH4, DVMCH5 → A0, A1, A2; EN ← +5V; (8C5) DVC0 → S1–S8; D → R58 100K

CAL IN → J104 → R57 1K → CR7 1N5282 (2) CR8 → -15V / +15V

+5V → C65 .1 → CR9 LM35DZ (V+, VOUT, GND) → TEMP (8C5)

+5V → R570 100K → U52 LT1013 1/2 (B); R104 6.04K; R105 95.3K

U36 ICL7109

C67 .1 (-5V); +5V → V+, CE/LOAD

(1C7) IOST1 → C69 220 pf; (B4) DVMOSC → OSC; R60 10K (NOM)

C72 .1 POLY; C71 .056 POLY; +2VREF (B1); R59 200K

R58 100K; C73 .01 POLY; C70 1 100v MYLAR

REFIN, BUF, HI IN, LO IN, RCAP, REFOUT, COMMON, GND

HIGH ORDER, LOW ORDER → AD7–AD0 (1D6)

RUN/HOLD → DVMRUN (1A1); LBEN → A2STB; HBEN → A3STB (1B3)

FREQUENCY COUNTER AND SELECT

C200 .1 +3V; RN3 150

U30 74ALS151 — (1C1) CTRCH0–CTRCH2 → A, B, C; EN; (8C5, 8B4) FRQ1–FRQ8 → D0–D7

R54 825; C58 470pf; R55 182; U31 CA3232 (IN, IN, OUT); R571 1K ← +5V; C59 1000pf SM; R56 40.2k

U32 74ALS151 — (1C1) CTRCH3–CTRCH5 → A, B, C; EN; (2C1) TRIGMEAS, (2A2) 10MOSC, (2C7) 10MCLK, (2D8) REFCLK, (D3) DVMOSC, INTTRIG (5B2) → D0–D7

U33 ST5152 — FRQ0 (8C5); AD0–AD7 (1D6); R/W, E, AS; CTRADY (1C8); SYSRST (8C8); CTR (1D3)

+2 VOLT REFERENCE

RN2: R1 8K, R2 2K; T912

+10VR (A6) → R63 100/20T → U29 LT1014 1/4 (C) → TP3 → +2VREF (D2)

+10 VOLT REFERENCE

+15V → U50 LT1021 (IN, OUT, GND) → U29 LT1014 1/4 (A)

R48 100; C56 220pf; R49 100; R47 15; Q4 2N2219A

+10VR (B2 2B6, 2A8, 5D4)

-10 VOLT REFERENCE

U51 LT1021 (IN, OUT, GND); C60 .1; R53 2.49K ← -15V

U29 LT1014 1/4 (B); R51 100; C57 220pf; R52 100; R50 15; Q5 2N2907A

-10VR (5D5)

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES | DRAWN R. SMITH / RO FIFER | DATE 2-20-90 | MATERIAL | PROJENGR | RELEASE APPROV | FINISH WAVETEK PROCESS | TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030 | DO NOT SCALE DWG | SCALE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: SCHEMATIC REF CAL

MODEL NO. 680 | DWG NO. 1104-00-3385 | REV C | CODE IDENT 23338 | SHEET 4 OF 8

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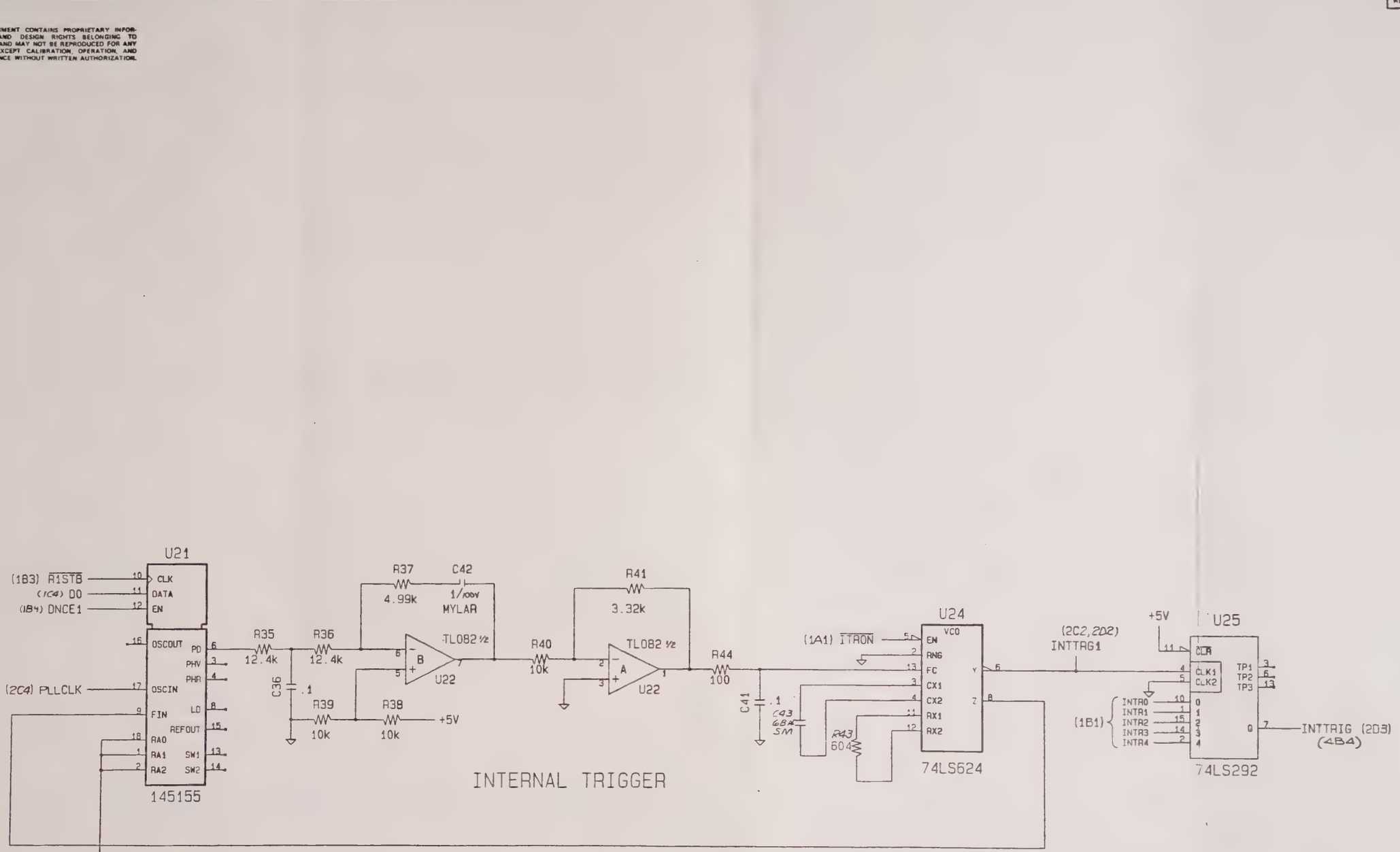
REV	ECN	BY	DATE	APP



NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN M SMITH 7/20/90
PROJ MGR
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ± .010 ANGLES ± 1° XX ± .030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE
SCHEMATIC
REF CAL

MODEL NO 680
DWG NO 1104-00-3385
REV C
CODE IDENT 23338
SHEET 5 OF 5

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REV	ECN	BY	DATE	APP

U37
(1B4) DACHI
CLK
OC
D7
D6
D5
D4
D3
D2
D1
D0
(1C4)
1D 2D 3D 4D 5D 6D 7D 8D
1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q
74ALS574

U38
(1B4) DACLO
CLK
OC
1D 2D 3D 4D 5D 6D 7D 8D
1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q
74ALS574

U41
TRIM
SJ
IOUT
IBPO
ADJ
V_OUT
RFB
PCM54
C132 .01

U39
(1B4) SHI
CLK
OC
1D 2D 3D 4D 5D 6D 7D 8D
1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q
74ALS574

+5V
R61 10K
R62 4.99K
-10V(7C7)

2N5486 Q6 — .1 POLY C96 — U42 A — RN5 10K — RN5 10K — C112 .01 — U43 A — 1/4TL084 — DAC7 (8D5)
1/4 LM339

2N5486 Q7 — .1 POLY C97 — U42 B — RN5 10K — RN5 10K — C113 .01 — U43 B — 1/4TL084 — DAC6 (8D4)
1/4 LM339

2N5486 Q8 — .1 POLY C98 — U42 C — RN5 10K — RN5 10K — C114 .01 — U43 C — 1/4TL084 — DAC5 (8D5)
1/4 LM339

2N5486 Q9 — .1 POLY C99 — U42 D — RN5 10K — RN5 10K — C80 .01 — U43 D — 1/4TL084 — DAC4 (8D4)
1/4 LM339

2N5486 Q10 — .1 POLY C100 — U44 A — RN6 10K — RN6 10K — C116 .01 — U45 A — 1/4TL084 — DAC3 (8D5)
1/4 LM339

DACV (7D7)

2N5486 Q11 — .1 POLY C101 — U44 B — RN6 10K — RN6 10K — C117 .01 — U45 B — 1/4TL084 — DAC2 (8D4)
1/4 LM339

1.67V (7D7)

2N5486 Q12 — .1 POLY C102 — U44 C — RN6 10K — RN6 10K — C118 .01 — U45 C — 1/4TL084 — DAC1 (8D5)
1/4 LM339

2N5486 Q13 — .1 POLY C103 — U44 D — RN6 10K — RN6 10K — C119 .01 — U45 D — 1/4TL084 — DAC0 (8D4)
1/4 LM339
-10V(7C7)

SAMPLE & HOLDS

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN R.DIFFER	DATE 2-20-90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC REF CAL
FINISH WAVETEK PROCESS	RELEASE APPROV	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030	
	DO NOT SCALE DWG	SCALE	MODEL NO. 680 · DWG NO. 1104-00-3385 · REV C
			CODE IDENT 23338 · SHEET 6 OF 8

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REV	ECN	BY	DATE	APP

(6C1)1.67V

(6C1) DACV

-15V — 1N751 CR10 — .1 C89 .01 C115

-10V A3,A6,6A2,6A5)

2N5486 Q14 — .1 POLY C104 — U46 1/4 LM339 — RN7 10K — RN7 10K — C120 .01 — U47 1/4 TL084 — DAC15 (8D5)

2N5486 Q15 — .1 POLY C105 — U46 1/4 LM339 — RN7 10K — RN7 10K — C121 .01 — U47 1/4 TL084 — DAC14 (8D5)

2N5486 Q16 — .1 POLY C106 — U46 1/4 LM339 — RN7 10K — RN7 10K — C122 .01 — U47 1/4 TL084 — DAC13 (8D5)

2N5486 Q17 — .1 POLY C107 — U46 1/4 LM339 (-10V (C7)) — RN7 10K — RN7 10K — C123 .01 — U47 1/4 TL084 — DAC12 (8D5)

U40 74ALS574
(1B4) SH2 → CLK, OC
(1C4) D7 D6 D5 D4 D3 D2 D1 D0

2N5486 Q18 — .1 POLY C108 — U48 1/4 LM339 — RN8 10K — RN8 10K — C124 .01 — U49 1/4 TL084 — DAC11 (8D5)

2N5486 Q19 — .1 POLY C109 — U48 1/4 LM339 — RN8 10K — RN8 10K — C125 .01 — U49 1/4 TL084 — DAC10 (8D5)

2N5486 Q20 — .1 POLY C110 — U48 1/4 LM339 — RN8 10K — RN8 10K — C126 .01 — U49 1/4 TL084 — DAC9 (8D5)

2N5486 Q21 — .1 POLY C111 — U48 1/4 LM339 (-10V (C7)) — RN8 10K — RN8 10K — C127 .01 — U49 1/4 TL084 — DAC8 (8D5)

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN RO FIFER
PROJ ENGR
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ± .010 ANGLES ±1° XX ± .030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC
REF CAL

MODEL NO. 680
DWG NO. 1104-00-3385
REV C
CODE IDENT 23338
SHEET 7 OF 8

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REV	ECN	BY	DATE	APP

BOARD EDGE CONNECTORS

J2

	A1	+3V	B1	-15V	C1
	A2	GND	B2	-2V	C2
	A3	GND	B3	-5V	C3
	A4	GND	B4		C4
GND	A5	GND	B5		C5
+5V	A6	+5V	B6	GND	C6
(1B5) LE	A7	(1B5) LA9	B7	-5V	C7
LA8	A8	LA7	B8	GND	C8
(1A5) LA6	A9	(1A5) LA5	B9		C9
LA4	A10	LA3	B10		C10
LA2	A11	LA1	B11	-2V	C11
GND	A12	+5V	B12		C12
LD7	A13	LD6	B13		C13
LD5	A14	(1A4) LD4	B14	GND	C14
(1A4) LD3	A15	LD2	B15		C15
LD1	A16	LD0	B16		C16
GND	A17	GND	B17	-2V	C17
(1A5) LR/W	A18	(1B5) CSRC	B18		C18
(1D4,4B2,1B6,1C8,2B3) SYSRST	A19	(1B5) AV2	B19		C19
+5V	A20	+5V	B20	-5V	C20
GND	A21	GND	B21	GND	C21
	A22	GND	B22		C22
	A23	GND	B23		C23
GND	A24	+5V	B24	(3B7) -2V	C24
(3B7,2D1) STRI6	A25	GND	B25	(2D1) STRI6	C25
GND	A26	GND	B26		C26
-2V	A27	GND	B27	GND	C27
	A28	GND	B28	(2C5) 10MHZ	C28
(2C5) 10MHZ	A29	GND	B29	10MHZ	C29
	A30	GND	B30	-5V	C30
(2C5) 10MHZ	A31	GND	B31	GND	C31
	A32	GND	B32	+15V	C32

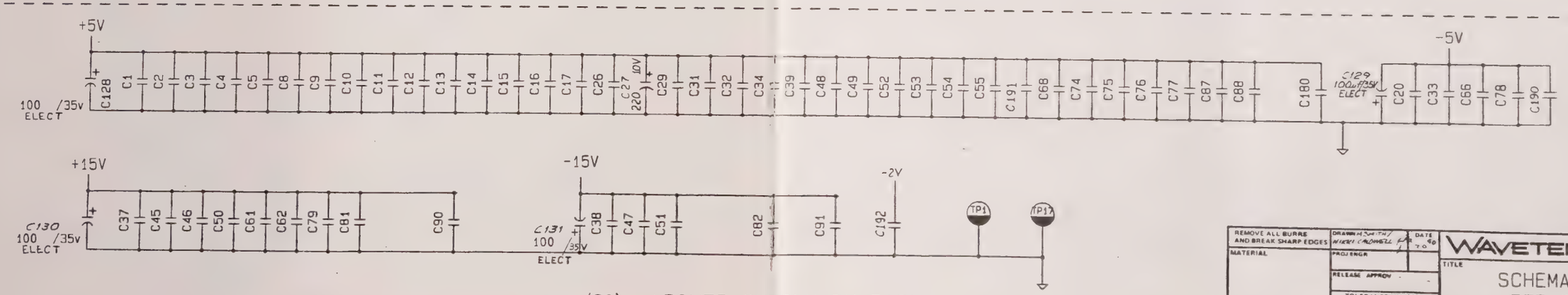
J1

-5V	A1	-5V	C1				
GND	A2	GND	C2				
+5V	A3	+5V	C3				
-2V	A4	-2V	C4				
GND	A5	GND	C5				
-5V	A6	-5V	C6				
GND	A7	GND	C7				
GND	A8	GND	C8				
(4A3) -10VR	A9	(4A6) -10VR	C9				
GND	A10	GND	C10				
(3B4) ANASUM	A11	(7B4) ANASUM	C11				
GND	A12	GND	C12				
(7D4) DAC15	A13	(7C4) DAC14	C13				
(7B4) DAC13	A14	(7B4) DAC12	C14				
(7D1) DAC11	A15	(7C1) DAC10	C15				
(7B1) DAC9	A16	(7A1) DAC8	C16				
(6D3) DAC7	A17	(6C3) DAC6	C17				
(6B3) DAC5	A18	(6B3) DAC4	C18				
(6D1) DAC3	A19	(6C1) DAC2	C19				
(6B1) DAC1	A20	(6B1) DAC0	C20				
GND	A21	GND	C21				
FRQ8	A22	FRQ7	C22				
FRQ6	A23	FRQ5	C23				
(4B8) FRQ4	A24	(4B8) FRQ3	C24				
FRQ2	A25	FRQ1	C25				
FRQ0	A26	FRQ0	C26				
(4C5) TEMP	A27	GND	C27				
(4C4) DCV0	A28	(REFCOM) GND	C28				
DCV8	A29	DCV7	C29				
(4D7) DCV6	A30	(4D7) DCV5	C30				
DVC4	A31	DCV3	C31				
DCV2	A32	DCV1	C32				

UNUSED GATES

REF DES	PART #	QTY UNUSED	GATE / PIN NUMBER
U20	10H124	3	7 1/4 3 1; 10 1/4 12 15; 11 1/4 13 14
U57	10116	1	13 12 1/3 14 15 11
U60	10H124	2	7 1/4 9 1; 5 1/4 4 2
U58	74LS32	3	4 5 6; 9 10 8; 12 13 11

	PART	27128	74ALS573	74LS138	6803	74LS86	68HC34	74LS139	74LS245	74ALS574	TCXO	NE521	74LS151	DNC2016	74LS74	10H12*	145155	TL082	74LS624	74LS292	DAC0832	LT1014	74ALS151	CA3232	ST5152	DG508	PCM54	LM339	TL084	LT1013	74LS157	74LS32
	GND	14	10	8	1	7	18	8	10	10	7	7	8	14, 17	7	16	7		1, 7	8	3, 10		8	5	6, 21	14	22				8	7
POWER	+5V	1, 27, 28	20	16	7	14	1	16	20	20	14	14	16	6, 18	14	9			9	16			16	2	40		26				16	14
SUPPLY	-5V											13				8											28					
	+15V																	8			19, 20	4				13		3	4	8		
	-15V																	4				11				3			11	4		
	REF DES	U1	U2, 3	U4, 9	U5	U6	U7	U8	U10	U11-13, U37-40	U14	U15, 17	U16, 23, 32	U18	U19	U20 U60	U21	U22, 27	U24	U25	U26	U29	U30	U31	U33	U34, 35	U41	U42, 44, 46, 48	U43, 45, 47, 49	U52	U54	U58



(60) .1 POWER SUPPLY BY PASS

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN M. SMITH / NIKKI CALDWELL	DATE 4-6-90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC REF CAL
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ± .010 ANGLES ±1° XX ± .03		MODEL NO. 680
	DO NOT SCALE DWG		DWG NO. 1104-00-3385 REV C
	SCALE		CODE IDENT 23338 SHEET 8 OF 8

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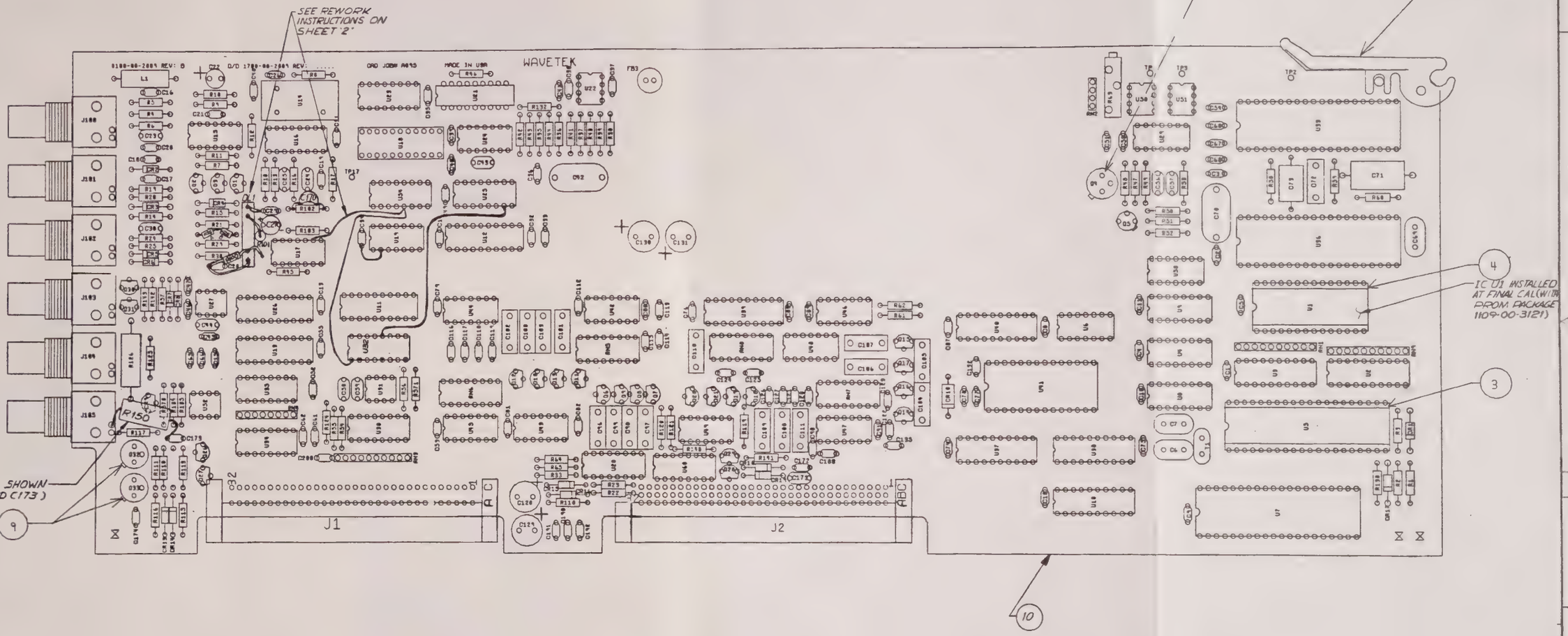
REV	ECN	BY	DATE	APP
A	ECO # 90-213	MS	2-20-90	



NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN M. Smith / RO FIFER	DATE 2-20-90	WAVETEK San Diego, California
MATERIAL	PROJ MGR		TITLE: ASSEMBLY REF CAL BOARD
FINISH WAVETEK PROCESS	RELEASE APPROV Tom Ball		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG	MODEL NO. 680	DWG NO. 1101-00-3385 REV A
	SCALE	CODE IDENT 23338	SHEET 1 OF 2

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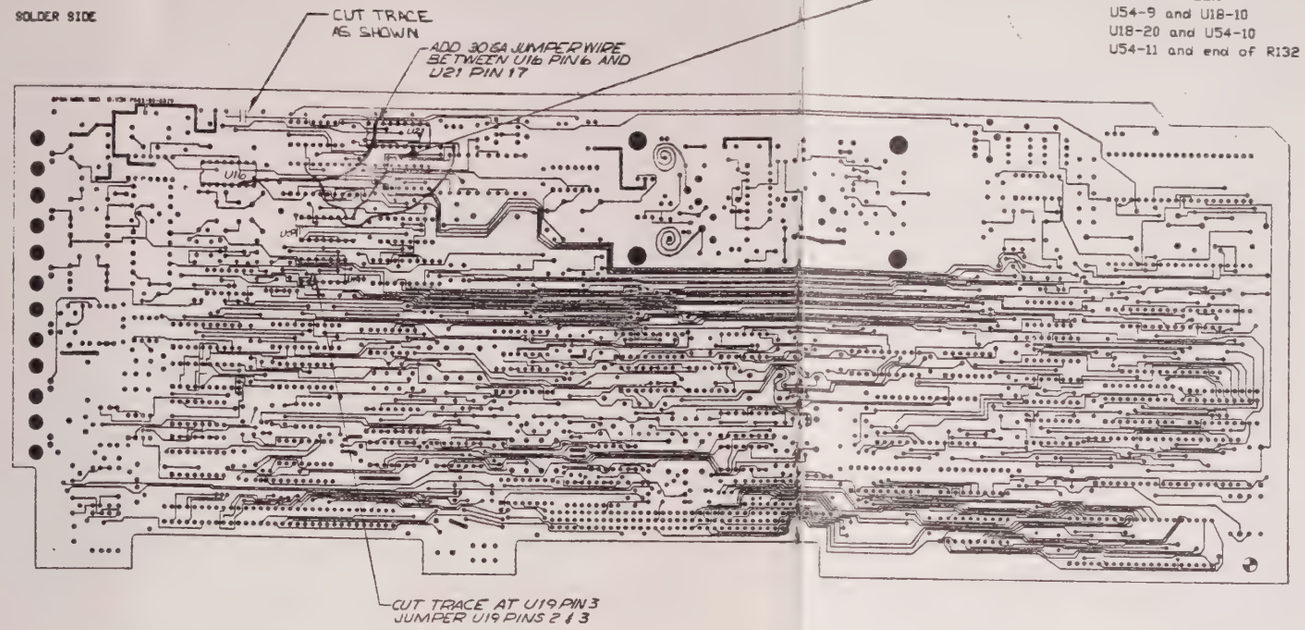
REV	ECN	BY	DATE	APP

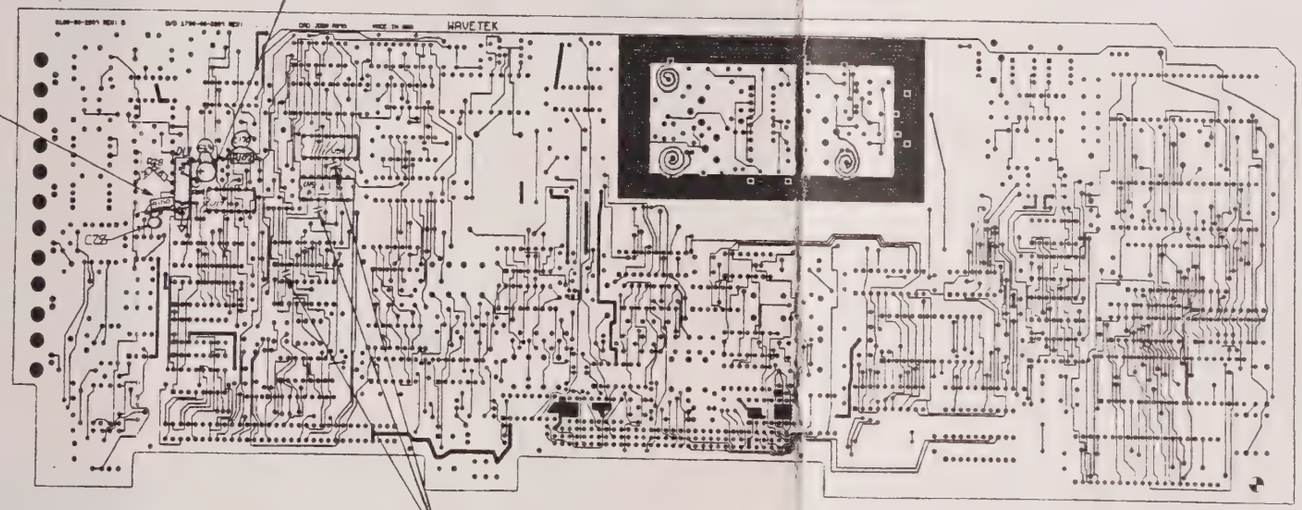
SOLDER SIDE


CUT TRACE AS SHOWN
ADD 30 GA JUMPER WIRE BETWEEN U16 PIN 6 AND U21 PIN 17
CUT ETCH ON SOLDER SIDE OF BOARD BETWEEN END OF R132 AND U18-10
INSTALL JUMPERS BETWEEN:
U54-9 and U18-10
U18-20 and U54-10
U54-11 and end of R132
CUT TRACE AT U19 PIN 3
JUMPER U19 PINS 2 & 3

TRACE CUT-REWORK INSTRUCTIONS
(SOLDER & COMPONENT SIDES)

1. CUT TRACE AT U19 PIN 3. COMPONENT SIDE AND SOLDER SIDE OF PCB.
2. DESOLDER AND LIFT, U19 PIN 2, OUT OF HOLE
3. BUSS PIN 2 & 3 OF U19 TOGETHER ON SOLDER SIDE OF BOARD
4. SOLDER 30 GA WIRE FROM U19 PIN 2 TO BOTTOM (GND) LEAD OF C34
5. CUT TRACE LOCATED BETWEEN PINS 15 AND 16 OF U32 ON COMPONENT SIDE.
6. CUT TRACE OF PIN 5 AT U54 ON COMPONENT SIDE OF PCB
7. SOLDER 30 GA WIRE FROM U32 PIN 1 TO U54 PIN 5
8. SOLDER 30 GA WIRE FROM U54 PIN 5 TO U17 PIN 9
9. CUT TRACE TO R8 ON SOLDER SIDE OF PCB.

COMPONENT SIDE



REWORK INSTRUCTIONS "DL1"

1. REMOVE R100, R101, C170
2. ADD DL1 UPSIDE DOWN (PINS FACING AWAY FROM BOARD) AND SOLDER JUMPER FROM "OUT" TO FEED THRU AS SHOWN.
3. ADD R100 FROM "OUT" TO C28 GND LEAD
4. ADD R101 (STANDUP) TO PAD FOR OLD R100 AND OPPOSITE END OF R101 TO "IN" OF DL1 AND SOLDER.
5. CONNECT GND (IN) PIN OF DL1 TO GND PAD OF C29 WITH #24 GA. WIRE. INSTALL BEFORE SOLDERING.
6. SOLDER JUMPER FROM GND LEAD OF C28 TO GND (OUT) PIN OF DL1 USING #24 GA. JUMPER WIRE WITH TEFLON TUBING INSULATION.
7. ADD C170 IN PARALLEL TO R102
8. REMOVE R28
9. ADD R28A AND R28B "IN SERIES" IN OLD R28 HOLES (AS SHOWN)

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN M. SMITH / RO FIFER	DATE 7-20-90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL —	PROJ ENGR		TITLE: ASSEMBLY, REF CAL BD (REWORK INSTRUCTIONS)
	RELEASE APPROV		
FINISH WAVETEK PROCESS —	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030		
	DO NOT SCALE DWG	MODEL NO. 680	DWG NO. 1101-00-33385 REV A
	SCALE —	CODE IDENT 23338	SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS

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REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRAWING PCA, REF CAL BOARD	1101-00-3385	WVTK	1101-00-3385	1
NONE	SCHEMATIC, REF CAL BOARD	1104-00-3385	WVTK	1104-00-3385	1
C112 C113 C114 C115 C116 C117 C118 C119 C120 C121 C122 C123 C124 C125 C126 C127 C132 C171 C28 C80	CAP, CER, MON, .01MF, 100 V	SR211E103ZAA	AVX	1500-00-1816	20
C1 C10 C11 C12 C13 C135 C14 C15 C16 C17 C170 C172 C173 C174 C18 C180 C19 C190 C191 C192 C2 C20 C200 C21 C210 C26 C29 C3 C31 C32 C33 C34 C35 C36 C37 C38 C39 C4 C40 C41 C43 C46 C47 C48 C49 C5 C50 C51 C52 C53 C54 C55 C60 C61 C62 C65 C66 C67 C68 C74 C73 C76 C77 C78 C79 C8 C81 C82 C87 C88 C89 C9 C90 C91	CAP CER MON .1MF 50V Z5U +80/-20% RAD LD SP .2 SP .2	SR215E104ZAA	AVX	1500-01-0420	74
C56 C57	CAP, CER, 220PF, 1KV	D221K20Z5FNAAEM	PHLIP	1500-02-2111	2
C44	CAP, CER, .22MF, 25V	CW30C224K	CRL	1500-02-2409	1
C30	CAP CER MON 2.7PF 50V	CCD2R7DNPO	ARCO	1500-02-7505	1
C24 C25	CAP, CER, 47PF, 1KV	DD-470	CRL	1500-04-7011	2
C23 C58	CAP, CER, 470PF, 1KV	DD-471	CRL	1500-04-7111	2

WAVETEK PARTS LIST | TITLE PCA, REF CAL BOARD | ASSEMBLY NO. 1100-00-3385 | REV B | PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C59	CAP MICA 1000PF 5% 100V RADIAL REF: 101.2100	DM15-102J	ARCO	1500-11-0200	1
C69	CAP, MICA, 220PF, 500V, RADIAL	DM15-221J	ARCO	1500-12-2100	1
C6 C7	CAP, MICA, 27PF, 500V	DM15-270J	ARCO	1500-12-7000	2
C43	CAP, MICA, 68PF, 500V	DM15-680J	ARCO	1500-16-8000	1
C22	CAP, ELECT, 10MF/25V RADIAL LEAD, SP .10	NRE 10/63	NIC	1500-31-0002	1
C128 C129 C130 C131	CAP, ELECT, 100MF, 35V RADIAL LEAD, SP .20	NRE101M35V10X12.5(DBS)	NIC	1500-31-0102	4
C27	CAP, ELECT, 220MF, 20%, 16V, RADIAL END MOUNT, 0.14 LEAD SPACE	16TWS220M	RUBY	1500-32-2104	1
C73	CAP, POLYC, .01MF, 100V AXIAL	C31B103F	BISHO	1500-41-0304	1
C100 C101 C102 C103 C104 C105 C106 C107 C108 C109 C110 C111 C72 C96 C97 C98 C99	CAP, MET POLY, .1mfd, 5%, 160v 0.1MFD 5%, 160V	171104J160D	MALRY	1500-41-0445	17
C42 C70	CAP, MYLAR, 1MF, 100V, RADIAL	PMT2R1.0K100	ITT	1500-41-0524	2
C71	CAP, POLYPRO, .056MF, 20	9A1C563-0	IMB	1500-43-6300	1

WAVETEK PARTS LIST | TITLE PCA, REF CAL BOARD | ASSEMBLY NO. 1100-00-3385 | REV B | PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
	0.05W, 2%, AXIAL				
10	DRILL DRWG, REF/CAL BD REF: SPEC 0008-00-0455 REV E	1700-00-2809	WVTK	1700-00-2809	1
L1	INDUCTOR, 390MH	2500-08	DELVN	1800-00-0023	1
DL1	DELAY LINE, 40 NSEC, 1000HM	1513-40B	DDD	1800-00-0039	1
J100 J101 J102 J103 J104 J105	CONN, BNC(PC)	227161-1	AMP	2100-01-0019	6
J1	CONN, DINMRT ANGLE, PC MOUNT, 64 PIN A&C LOAD ROWS, 0.1 SPACING	D3M064RA27D8	HOLM	2100-02-0220	1
J2	CONN, DIN, MALE, 96 PIN, A/B/C, RTA	P196B30P00F00Z1	BURND	2100-02-0236	1
3	SKT, IC, 40PIN	DILB40P-108T	BURND	2100-03-0030	1
4	SKT, IC, 28PIN	DILB28P-108T	BURND	2100-03-0055	1
TP1 TP17 TP2 TP3 TP4	TEST POINT, PC-TYPE	2100-04-0055	WVTK	2100-05-0024	5
Y1	CRYSTAL, 4MHZ	180-502	MTRON	2300-99-0004	1
U14	OSCILLATOR, TEMP COMPENSATED 10MHZ XTAL, 14 PIN DIP,	7400B2A1	MONIT	2300-99-0026	1

WAVETEK PARTS LIST | TITLE PCA, REF CAL BOARD | ASSEMBLY NO. 1100-00-3385 | REV B | PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	0.030 LEADS				
6	PC BD EJECTOR	87-2-C	BRIT	2900-07-0032	1
9	TRANSIPAD	1D123N(DBS)	METRS	2900-11-0003	3
FB3	BALUN CORE	2B73000902	FARIT	3100-00-0002	1
R63	POT, TRIM, 20T, 100	43P101	SPECT	4600-11-0100	1
R100 R101 R117 R118 R33 R44 R48 R49 R51 R52 R7	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	12
R11 R12 R57 R571 R6	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	5
R10 R130 R132 R2 R3 R30 R39 R40 R60T R61	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	11
R570 R58	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	2
R42 R46	RES, MF, 1/8W, 1%, 10	3043ED10R100F	MEPCO	4701-03-1009	2
R103	RES, MF, 1/8W, 1%, 10.5K	RN55D-1052F	TRW	4701-03-1052	1
R17	RES, MF, 1/8W, 1%, 1.21K	RN55D-1211F	TRW	4701-03-1211	1
R24 R35 R36	RES, MF, 1/8W, 1%, 12.4K	RN55D-1242F	TRW	4701-03-1242	3
R113 R115	RES, MF, 1/8W, 1%, 150	RN55D-1500F	TRW	4701-03-1500	2
R45	RES, MF, 1/8W, 1%, 150K	RN55D-1503F	TRW	4701-03-1503	1
R47 R50	RES, MF, 1/8W, 1%, 15	RN55D-15R0F	TRW	4701-03-1509	2

WAVETEK PARTS LIST | TITLE PCA, REF CAL BOARD | ASSEMBLY NO. 1100-00-3385 | REV B | PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R55	RES, MF, 1/8W, 1%, 182	RN55D-1820F	TRW	4701-03-1820	1
R288	RES, MF, 1/8W, 1%, 200	RN55D-2000F	TRW	4701-03-2000	1
R102	RES, MF, 1/8W, 1%, 2K	RN55D-2001F	TRW	4701-03-2001	1
R28A	RES, MF, 1/8W, 1%, 20K	RN55D-2002F	TRW	4701-03-2002	1
R59	RES, MF, 1/8W, 1%, 200K	RN55D-2003F	MEPCO	4701-03-2003	1
R125 R142 R143	RES, MF, 1/8W, 1%, 21.5	RN55D-21R5F	TRW	4701-03-2159	3
R21	RES, MF, 1/8W, 1%, 249	RN55D-2490F	TRW	4701-03-2490	1
R116 R53	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	2
R64 R65	RES, MF, 1/8W, 1%, 301	RN55D-3010F	TRW	4701-03-3010	2
R25	RES, MF, 1/8W, 1%, 3.01K	RN55D-3011F	TRW	4701-03-3011	1
R110 R111	RES, MF, 1/8W, 1%, 316	RN55D-3160F	TRW	4701-03-3160	2
R119	RES, MF, 1/8W, 1%, 332	RN55D-3320F	TRW	4701-03-3320	1
R1 R41	RES, MF, 1/8W, 1%, 3.32K	RN55D-3321F	TRW	4701-03-3321	2
R56 R9	RES, MF, 1/8W, 1%, 40.2K	RN55D-4022F	TRW	4701-03-4022	2
R120 R140 R141 R19 R20	RES, MF, 1.0W, 1%, 46.4	RN55D-46R4F	TRW	4701-03-4649	5
R14 R15 R8	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	3

WAVETEK PARTS LIST | TITLE PCA, REF CAL BOARD | ASSEMBLY NO. 1100-00-3385 | REV B | PAGE 5

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R29 R37 R5 R62	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	4
R22 R23	RES, MF, 1/8W, 1%, 49.9	RN55D-49R9F	CORNO	4701-03-4999	2
R124	RES, MF, 1/8W, 1%, 51.1	RN55D-51R1F	TRW	4701-03-5119	1
R43	RES, MF, 1/8W, 1%, 604	RN55D-6040F	TRW	4701-03-6040	1
R104	RES, MF, 1/8W, 1%, 6.04K	RN55D-6041F	MEPCO	4701-03-6041	1
R13	RES, MF, 1/8W, 1%, 750	RN55D-7500F	TRW	4701-03-7500	1
R16 R18 R54	RES, MF, 1/8W, 1%, 825	RN55D-8250F	TRW	4701-03-8250	3
R121	RES, MF, 1/8W, 1%, 82.5	RN55D-82R5F	TRW	4701-03-8259	1
R105	RES, MF, 1/8W, 1%, 95.3K	RN55D-9532F	TRW	4701-03-9532	1
R126 R150	RES, MF, 1/2W, 1%, 49.9	RN65D-49R9F	TRW	4701-23-4999	2
RN1 RN9	RES NETWORK 2.2K 2% 10 PIN SIP BUSS	4310R-101-222	BOURN	4770-00-0011	2
RN4	RES NETWORK QUAD 8PIN SIP	T914-5K-020-05	CADDO	4770-00-0049	1
RN2	RES NETWORK, 10V TO 2V DIVIDER, 4-PIN SIP, 0.1 SPACE	T912-254	CADDO	4770-00-0050	1
RN3	RES NETWORK, 10 PIN SIP 150 OHM BUSS	4310R-101-151	BOURN	4770-00-0051	1

WAVETEK PARTS LIST | TITLE PCA, REF CAL BOARD | ASSEMBLY NO. 1100-00-3385 | REV B | PAGE 6

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES | MATERIAL | FINISH WAVETEK PROCESS | DRAWN | DATE | CHECKED | PROJ ENGR | RELEASE APPROV | UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± .XXX ± ° | DO NOT SCALE DRAWING

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: PARTS LIST REF/CAL BOARD

SIZE	FSCM NO	DWG. NO.	REV
D	23338	1100-00-3385	B

SCALE | MODEL 869 | SHEET 1 OF 2

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REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
RN3 RN6 RN7 RN8	RES NETWORK 8-RESISTORS, 16 PIN DIP ISOL	4116R-001-10K	BOURN	4770-00-0052	4
CR10	DIODE, ZENOR, 3.1V, 500MW, GIB, IN751A	1N751A	FAIR	4801-01-0751	1
CR13 CR14	DIODE, ZENER, 7.5V, IN755	1N755A	MOT	4801-01-0755	2
CR5 CR6 CR7 CR8	DIODE, HIGH CONDUCTANCE, ULTRA FAST	1N5282	FAIR	4801-01-5282	4
CR2	DIODE 1N4148 COMPUTER, G/P, 75V, 200M A, SWITCHING	1N4148	NSC	4807-02-6666	1
CR1 CR15 CR16 CR17 CR18 CR19 CR3 CR4	DIODE 5082-2811 SCHOTTKY, 15V, 20MA	5082-2811	HP	4809-02-2811	8
Q33 Q4	TRANS 2N2219A NPN GENERAL PURPOSE TO-5	2N2219A	NSC	4901-02-2191	2
Q32	TRANS 2N2905A PNP GENERAL PURPOSE TO-5	2N2905A	NSC	4901-02-9051	1
Q5	TRANS, METAL CAN	2N2907A	NAT	4901-02-9071	1
Q28 Q29	TRANS, NPN, TO-92	PN3563	NSC	4901-03-5630	2
Q1 Q27 Q3	TRANS 2N3904 NPN GENERAL PURPOSE TO-92	2N3904	FAIR	4901-03-9040	3

WAVETEK PARTS LIST | TITLE PCA, REF CAL BOARD | ASSEMBLY NO. 1100-00-3385 | REV B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
Q2 Q26	TRANS 2N3906 PNP GENERAL PURPOSE TO-92	2N3906(OBS)	FAIR	4901-03-9060	2
Q10 Q11 Q12 Q13 Q14 Q15 Q16 Q17 Q18 Q19 Q20 Q21 Q6 Q7 Q8 Q9	TRANS N-CHANNEL JFETS	2N5486	MOT	4901-05-4860	16
Q30 Q31	TRANS 2N5771 PNP SWITCH TO-92	2N5771	NSC	4901-05-7710	2
NONE	WIRE, HU, 20GA, WHITE	H0101018 (WHT)	JUDD	6000-32-0009	1
NONE	WIRE, WIRE WRAP, WHITE, 30AWG	UL1422 WHT 30GA	BRDRX	6000-53-0009	1
CR9	CENTIGRADE TEMP SENSOR	LM35DZ	NAT	7000-00-3500	1
U41	DAC, 16 BIT, INT REF, 28 PIN DIP	PCM54HP	BURR	7000-00-5401	1
U43 U45 U47 U49	OP AMP, QUAD BIMOS MOS/FET INPUT	TL084CN	TI	7000-00-8400	4
U42 U44 U46 U48	COMPARATORS, QUAD VOLTAGE	LM339N	HARIS	7000-03-3900	4
U34 U35	MUX, CMOS, D 4C, 8 CHAN/DUAL 4 CHAN ANAL	DG508ACJ	SLCON	7000-05-0800	2
U15 U17	COMPARATOR, DUAL DIFFERENTIAL, SENSE	NE521N	SIG	7000-05-2100	2

WAVETEK PARTS LIST | TITLE PCA, REF CAL BOARD | ASSEMBLY NO. 1100-00-3385 | REV B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	AMP				
U22 U27	OP AMP INPUT	TL082CP	TI	7000-08-2000	2
U26	DAC, LIN, CMOS, 8 BIT	DAC0832LCN	NSC	7000-08-3200	1
U52	OP AMP, DUAL PRECISION, 8-PIN DIP	LT1013CN8	LINTE	7000-10-1301	1
U29	OP-AMP QUAD, 14 PIN DIP	LT1014DN	LINTE	7000-10-1401	1
U50 U51	VOLTAGE REFERENCE, 10V, 8 PIN DIP	LT1021CCN8-10	LINTE	7000-10-2101	2
U36	ADC, 12 BIT	ICL7109CPL	INTSL	7000-71-0900	1
U31	COUNTER, DIVIDE BY 20 PRESCALER, 200MHZ, OPEN COLLECTOR, 8 PIN DIP	CA3232E	RCA	8000-32-3201	1
U5	MICROPROCESSOR, 8BIT	EF6803P	SGS	8000-68-0300	1
U58	GATE, OR, QUAD 2INP, TTL	N74LS32N	SIG	8000-74-3210	1
U19	FLIP-FLOP DUAL, D-POS EDGE TRIG, TTL	SN74LS74AN	TI	8000-74-7410	1
U6	GATE XOR, QUAD 2INP, TTL	74LS86	TI	8000-74-8610	1

WAVETEK PARTS LIST | TITLE PCA, REF CAL BOARD | ASSEMBLY NO. 1100-00-3385 | REV B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U20 U60	TRANSLATOR, QUAD TTL-TO-MECL	MC10H124P	MOT	8001-01-2401	2
U4 U9	DECODER, 1-8 LINE, TTL	74LS138	TI	8007-41-3810	2
U8	DECODER, DUAL 2-4, TTL	74LS139	SIG	8007-41-3910	1
U23 U30 U32	DATA SELECTOR/MUX, ADV LO PWR SCHOTTKY, 16-PIN DIP	SN74ALS151N/J(NO BUY)	MOT	8007-41-5111	3
U16	MUX, 8 INP, CMOS	SN74HC151N	TI	8007-41-5140	1
U54	MUX, QUAD, 2-INP, TTL	SN74LS157N	TI	8007-41-5710	1
U10	XCVR, OCT BUS, TTL	74LS245	TI	8007-42-4510	1
U25	PROG DIV/TIMER, TTL	74LS292	TI	8007-42-9210	1
U2 U3	LATCH, OCTAL D	SN74ALS573CN	TI	8007-45-7310	2
U11 U12 U13 U37 U38 U39 U40	FLIP-FLOP, OCTAL D	SN74ALS574N	TI	8007-45-7450	7
U24	VCO, TTL	74LS624	TI	8007-46-2410	1
U21	SYNTH, PLL FREQ, CMOS	MC145155P2	MOT	8100-00-0007	1
U1	EPROM PROG, USES 1 EA., 8002-71-2800	8600-00-0586	WAVTK	8600-00-0586	1
U18	GATE ARRAY, COUNTER, SYNCH, M ULTI-MODE, 32-BIT	CLA53047/BW/DP	PLESS	8700-00-0005	1

WAVETEK PARTS LIST | TITLE PCA, REF CAL BOARD | ASSEMBLY NO. 1100-00-3385 | REV B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U33	LSI, CUSTOM GATE ARRAY, CMOS, 4 CHAN UNIV COUNTER/TIMER	8700-51-5201	WVTK	8700-51-5201	1
U7	RAM, DUAL PORT, HCMOS, 40PIN DIP, PLASTIC	XC68HC34P	MOT	8900-68-3401	1

WAVETEK PARTS LIST | TITLE PCA, REF CAL BOARD | ASSEMBLY NO. 1100-00-3385 | REV B

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: PARTS LIST REF/CAL BOARD
	PROJ. ENGR.		
	RELEASE APPROV.		
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1100-00-3385 · REV B
DO NOT SCALE DRAWING			SCALE · MODEL 869 · SHEET 2 OF

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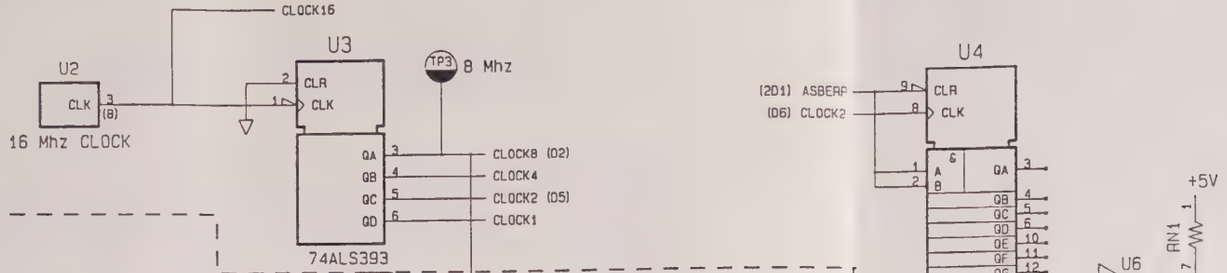
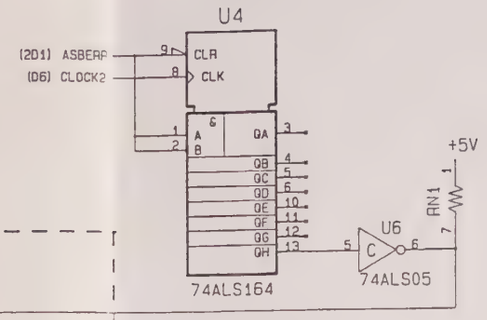
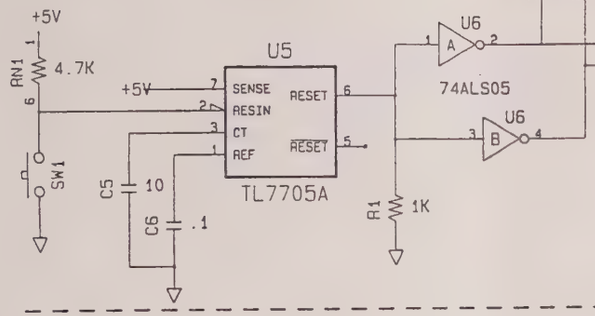
REV	ECN	BY	DATE	APP
A	REDRAWN USING 0103-00-3127 BY S.C ERO 90-434	SC	4-11-90	K.Ho

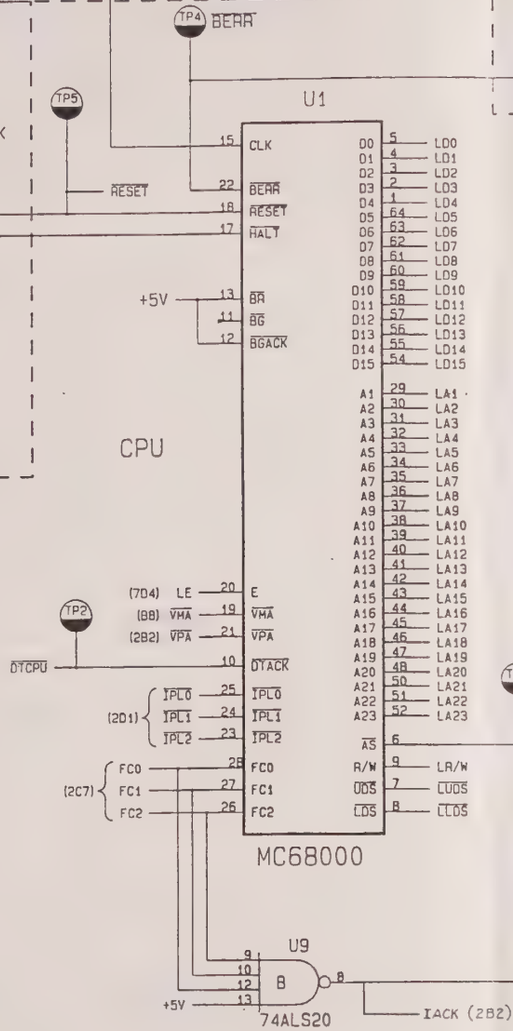
CLOCK



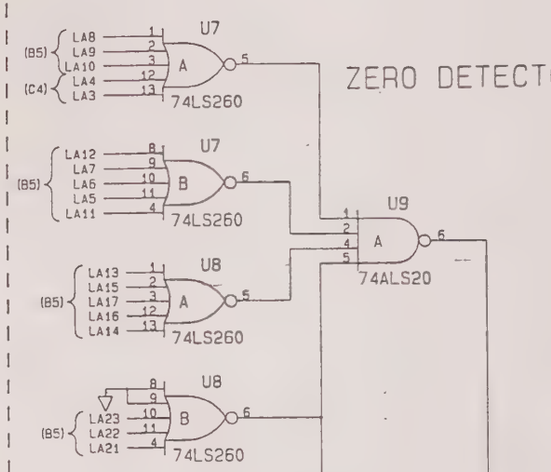


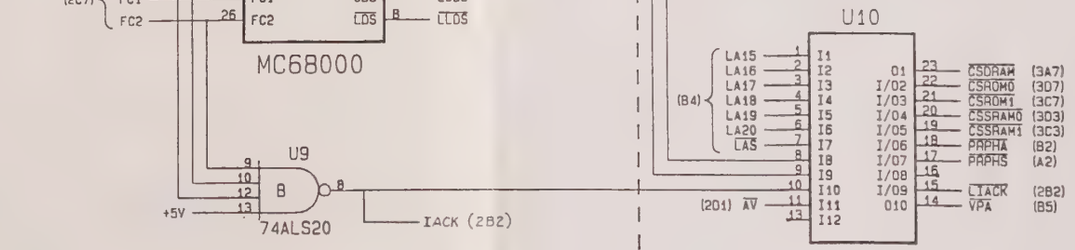
RESET



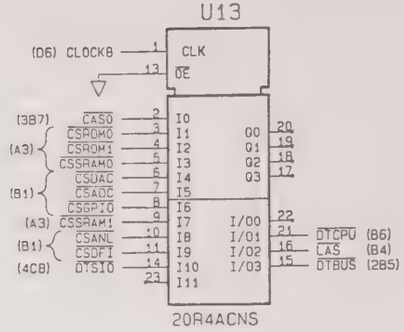


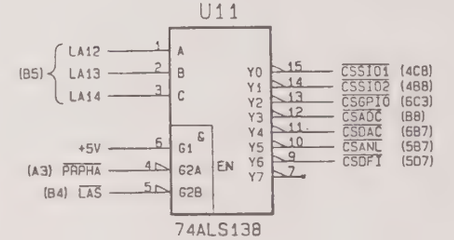
ZERO DETECTOR

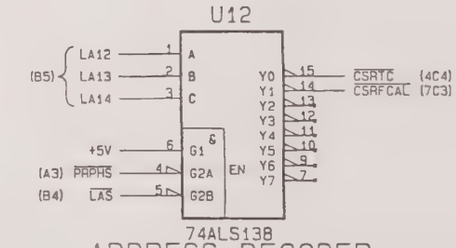




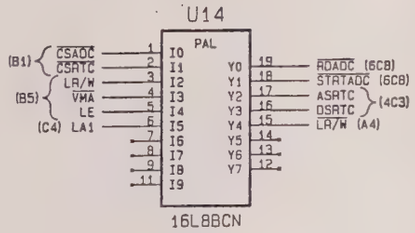
DTACK







ADDRESS DECODER



2. ALL CAPACITORS ARE IN MICROFARADS
1. ALL RESISTORS ARE OHMS 1%, 1/8W, MF

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN JQK/DMB	DATE 5/23/89	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENG Kurt Ho	742-90	TITLE SCHEMATIC 68000 VME
FINISH WAVETEK PROCESS	RELEASE APPROV Kurt Ho		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG SCALE	MODEL NO. 869	DWG NO. 1104-00-3409 REV A
		CODE IDENT 23338	SHEET 1 OF 7

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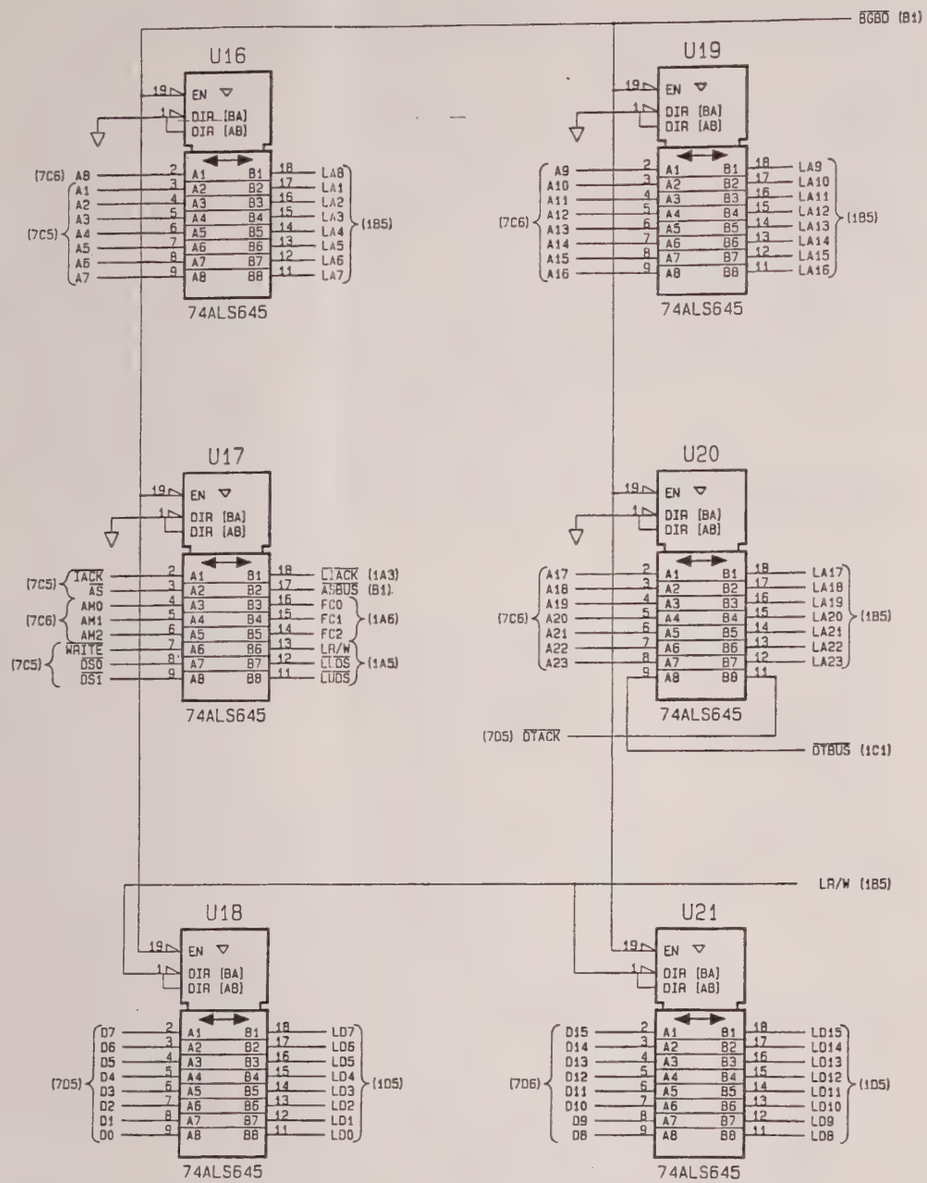
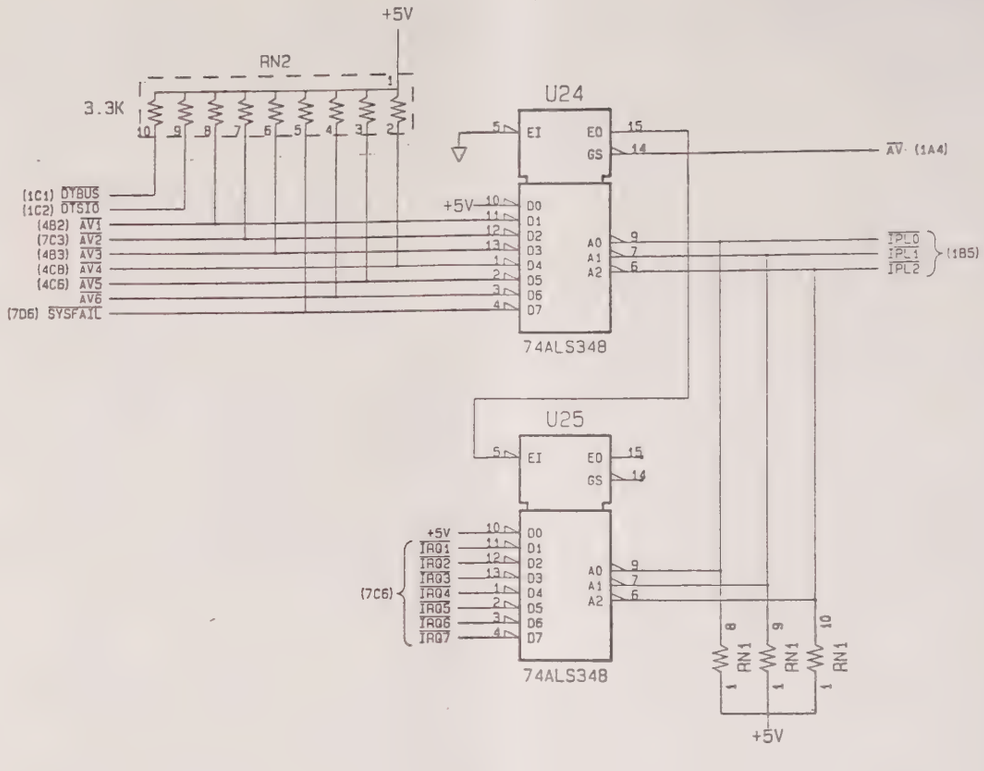
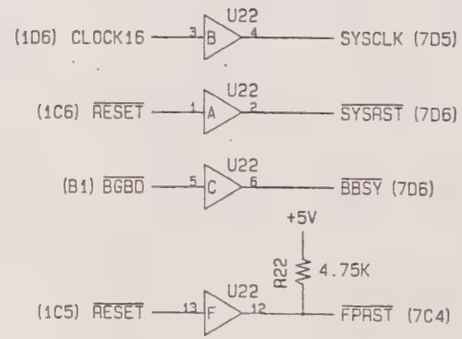
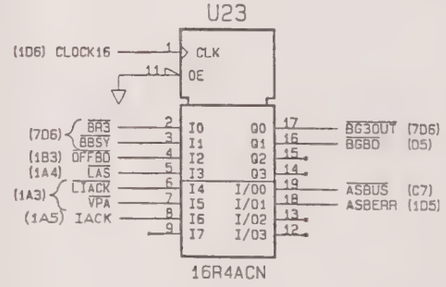
VME INTERFACE



NOTE: UNLESS OTHERWISE SPECIFIED







VME BUS ARBITRATION

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN JDK/DMB	DATE 6/1/88	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR Ed Reyes	6/1/88	TITLE SCHEMATIC 68000 VME
FINISH WAVETEK PROCESS	RELEASE APPROVED		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 869 / DWG NO. 1104-00-3409 / REV A
	SCALE		CODE IDENT 23338 / SHEET 2 OF 7

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REV	ECN	BY	DATE	APP

SYSTEM FIRMWARE
(4) 27512/27010 (64KX8/128KX8)

U26 — (1A3) CSROM0, (1B5) LLDS, +5V, VPP, PGM, OE, CE, LA1–LA17, LD0–LD7 (1C5)

U27 — (1B5) LUDS, +5V, VPP, PGM, OE, CE, LA1–LA17, LD8–LD15 (1C5)

U28 — (1A3) CSROM1, +5V, VPP, PGM, OE, CE, LA1–LA17, LD0–LD7 (1C5)

U29 — +5V, VPP, PGM, OE, CE, LA1–LA17, LD8–LD15 (1C5)

OPTIONAL EXTENDED MEMORY

U30 — (1A3) CSSRAM0, (1A5) LLDS, OE, CS, WE, LA1–LA14, (1B5), LD0–LD7 (1C5), DS1230

U31 — (1A5) LUDS, OE, CS, WE, LA1–LA14, (1B5), LD8–LD15 (1C5), DS1230

R30A — (1B5) LA15 — 10

R30B — +5V — 10

U32 — (1A3) CSSRAM1, (1A5) LLDS, OE, CS, WE, LA1–LA14, (1B5), LD0–LD7 (1C5), DS1230

U34 — 74F32 — (1A5) LR/W

U33 — (1A5) LUDS, OE, CS, WE, LA1–LA14, (1B5), LD8–LD15 (1C5), DS1230

U34 — 74F32 — (1A5) LR/W

R32A — (1B5) LA15 — 10

R32B — +5V — 10

INSTALL R30A AND R32A FOR 32K X 8
INSTALL R30B AND R32B FOR 8K X 8

NONVOLATILE STATIC RAM

DYNAMIC RAM

U35 — 4502 — (1B5) LA1–LA9, LA10–LA18, (1A4) LAS, (1A3) CSDRAM, +5V, (1C6) RESET, (1D6) CLOCKB, MA0–MA8, RAS0, RAS1, RAS2, RAS3, CAS0, CAS1, RDY

(TP39) RAS

R35 — 33.2

R36 — 33.2

U36 — MH25608JA-15 — (1B5) LR/W, RAS, CAS, W, (A6) MA0–MA8, DQ0–DQ7 (1C5)

U34 — 74F32 — (1B5) LLDS, (1C2) CAS0, (1B5) LUDS

R37 — 33.2

U37 — MH25608JA-15 — (1B5) LR/W, RAS, CAS, W, (A6) MA0–MA8, DQ0–DQ7 (1C5)

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN J.D.K./D.M.B. DATE 3/27/91
PROJENGR Ed Rains 4/96
RELEASE APPROV. Bill Hill
TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: SCHEMATIC 68000 VME

MODEL NO 869 | DWG NO. 1104-00-3409 | REV A
CODE IDENT 23338 | SHEET 3 OF 7

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REV	ECN	BY	DATE	APP

SERIAL I/O PORTS

U40 68681 — C46 15pf; Y40 3.6864 MHz; C47 5pf; TP40 125 Khz; U46 C; FPTX, FPRX (704); FPCLK (704); AV5 (2D3); LD0–LD7 (1C5); LA1–LA4; R/W (1C6); CSSIO1 (1B1); DTSIO (1C2); AV4 (2D3); +5V; RESET (1C6)

U41 68681 — FOR TEST ONLY — TP41 3.6864 Mhz; U46 74ALS1004; CSSIO2 (1B1); AV3 (2D3); +5V

U42 MC1488; U43 MC1489; U42 MC1488

P3 MONITOR

U44 MC1488; U45 MC1489; U45 MC1489; U44 MC1488

P1 TERMINAL

U44 MC1488; U45 MC1489; U45 MC1489; U44 MC1488

P2 HOST

NOTE: UNLESS OTHERWISE SPECIFIED

REAL TIME CLOCK

+5V; CR1 MBR120; +5SBY; CR2 HP2811

U49 74ALS645 — (1B1) CSRTC; (1A5) LR/W; LD0–LD7 (1C5); ASRTC; DSRTC; LR/W (1B7)

U50 146818 — TP50 32.768 Khz; C51 33pf NPO; R50 150K; C52 33pf NPO; Y50 32.768Khz; R51 5.6M; C53 15pf NPO; R52 2K; C54 .005; RESET (1C5); AV1 (2D3)

U6 74ALS05 — (1C5) RESET; R53 10K

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN JDK/DMB	DATE 9/2/88	WAVETEK San Diego, California
MATERIAL	PROJ ENGR Ed Ramos 9/88		TITLE SCHEMATIC 68000 VME
FINISH WAVETEK PROCESS	RELEASE APPROV Dale Wheeler		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 869
	SCALE		DWG NO. 1104-00-3409 REV A
			CODE IDENT 23338 SHEET 4 OF —

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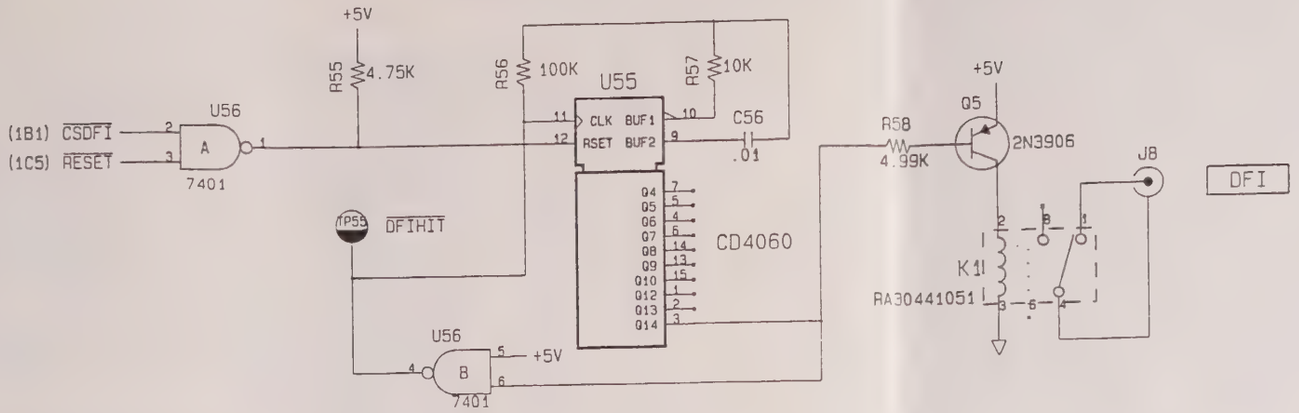
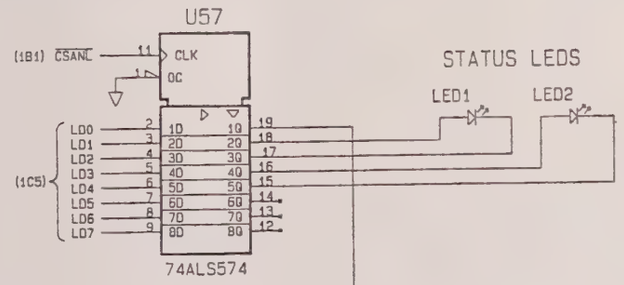
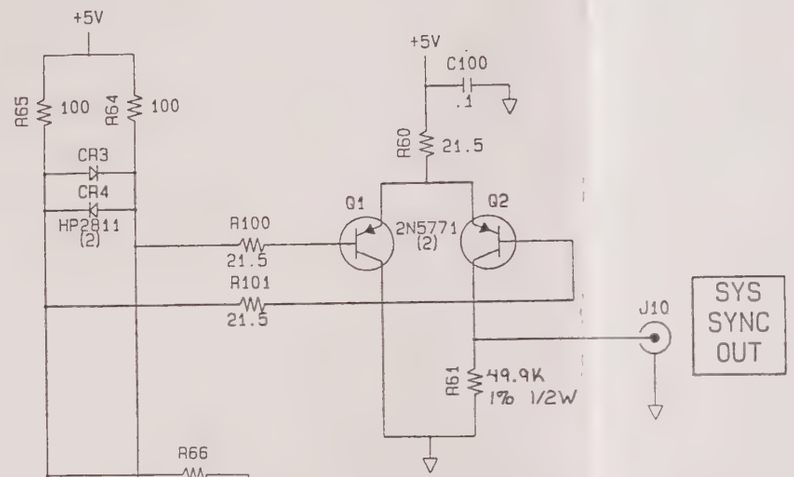
REV	FCN	BY	DATE	APP

DYNAMIC FAULT INDICATOR







NOTE. UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN J.DK/DMB 6/23/88	WAVETEK SAN DIEGO, CALIFORNIA	
MATERIAL	PROJ ENGR E. Reyes 6/88	TITLE SCHEMATIC 68000 VME	
FINISH WAVETEK PROCESS	RELEASE APPROVAL		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG	MODEL NO. 869	DWG NO. 1104-00-3409 REV A
	SCALE	CODE IDENT 23338	SHEET 5 OF 7

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REV	ECN	BY	DATE	APP

P27

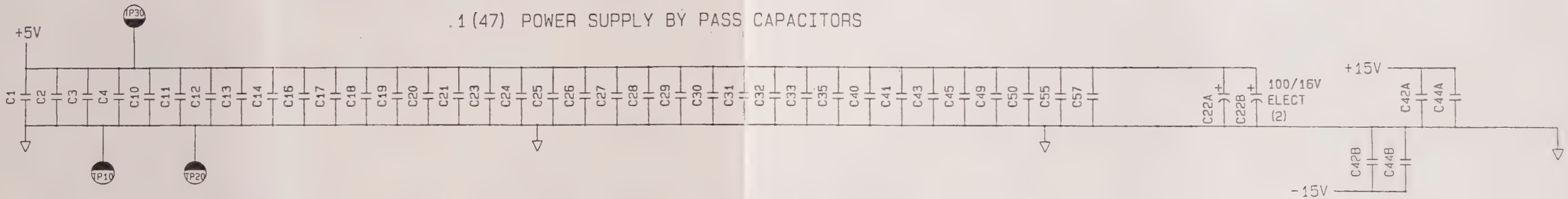
C1	D8	B1	BBSY	A1	D0
C2	D9	B2		A2	D1
C3	D10	B3		A3	D2
C4	D11	B4	BG0	A4	D3
C5	D12	B5		A5	D4
C6	D13	B6	BG1	A6	D5
C7	D14	B7		A7	D6
C8	D15	B8	BG2	A8	D7
C9	GND	B9		A9	GND
C10	SYSFAIL	B10	BG3IN	A10	SYSCLK
C11	BERR	B11	BG3OUT	A11	GND
C12	SYSRST	B12		A12	DS1
C13		B13		A13	DS0
C14	+5V	B14		A14	WRITE
C15	A23	B15	BR3	A15	GND
C16	A22	B16	AM0	A16	DTACK
C17	A21	B17	AM1	A17	
C18	A20	B18	AM2	A18	AS
C19	A19	B19	+5V	A19	GND
C20	A18	B20	GND	A20	
C21	A17	B21		A21	IACK
C22	A16	B22		A22	
C23	A15	B23	GND	A23	+5V
C24	A14	B24	IRQ7	A24	A7
C25	A13	B25	IRQ6	A25	A6
C26	A12	B26	IRQ5	A26	A5
C27	A11	B27	IRQ4	A27	A4
C28	A10	B28	IRQ3	A28	A3
C29	A9	B29	IRQ2	A29	A2
C30	A8	B30	IRQ1	A30	A1
C31		B31	+5SBY	A31	
C32	+5V	B32	+5V	A32	+5V

VME CONNECTOR

P28

GND	A1	-15V	C1
FPCLK	A2	-15V	C2
FPRX	A3	-5V	C3
FPTX	A4	GND	C4
GND	A5	+5V	C5
+5V	A6	GND	C6
LE	A7	LA9	C7
LA8	A8	LA7	C8
LA6	A9	LA5	C9
LA4	A10	LA3	C10
LA2	A11	LA1	C11
GND	A12	+5V	C12
LD7	A13	LD6	C13
LD5	A14	LD4	C14
LD3	A15	LD2	C15
LD1	A16	LD0	C16
GND	A17	GND	C17
LR/W	A18	CSAFCAL	C18
FPRST	A19	AV2	C19
-2V	A20	+5V	C20
GND	A21	GND	C21
SSYNC	A22	SSYNC	C22
SSYNC	A23	SSYNC	C23
GND	A24	-2V	C24
STRIG	A25	STRIG	C25
STRIG	A26	STRIG	C26
GND	A27	GND	C27
-2V	A28	-5V	C28
-5V	A29	+5V	C29
GND	A30	GND	C30
+5V	A31	+15V	C31
GND	A32	+15V	C32

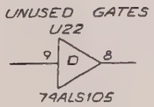
.1 (47) POWER SUPPLY BY PASS CAPACITORS



REF DES	U1	U2	U3	U4	U5	U6	U7, 8	U9	U10	U11, 12	U13	U14	U16-21, 49	U22	U23	U24, 25	U26-29
GND	16, 53	7	7	7	4	7	7	7	12	8	12	10	10	7	10	8	16
+5V	14, 49	14	14	14	8	14	14	14	24	16	24	20	20	14	20	16	30, 32
	68000	CLK	74ALS393	74ALS164	TL7705A	74ALS05	74LS260	74ALS20	20L10B	74ALS138	20P4A	16L8	74ALS645-1	74ALS1035	16R4	74ALS348	27010 27512

REF DES	U30, 33	U34	U35	U36, 37	U40, 41	U42, 44	U43, 45	U46	U55	U56	U57	U58
GND	14	7	35	9	20	7	7	7	8	7	10	15
+5V	28	14	37	1, 30	40		14	14	16	14	20	9
-5V												8
+15V						14						
-15V						1						
	DS1230	74F32	4502	MH25608	68681	1488	1489	74ALS1004	4060	7401	74ALS574	10H124

UNUSED GATES



POWER SUPPLY HOOK UP TABLES

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN J.D.K/D.M.B.	DATE 5/23/88	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR Ed Reuss	5/88	TITLE SCHEMATIC 68000 VME
FINISH WAVETEK PROCESS	RELEASE APPROV	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030	
	DO NOT SCALE DWG		
	SCALE	MODEL NO. 869	DWG NO. 1104-00-3409 REV A
		CODE IDENT 23338	SHEET 6 OF 7

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REV	ECN	BY	DATE	APP

VMEbus signals

A1 - A23	VMEbus address lines from the VME bus drivers
D1 - D15	VMEbus data lines from the VME bus drivers
IACK*	VMEbus interrupt acknowledge
AS*	VMEbus address strobe
DS0*	VMEbus Data Strobe 0
DS1*	VMEbus Data Strobe 1
WRITE*	VMEbus write signal
AM0 - 2	VMEbus address modifier signals
SYSCLK	VMEbus system clock signal. 16MHz
SYSRST*	VMEbus system reset signal
IRQ1-7*	VMEbus interrupt request lines
BG3OUT*	VMEbus Bus Grant 3 signal
BERR*	Bus Error input from the VMEbus
SYSFAIL*	Sysfail input from the VMEbus
DTACK*	Data Transfer Acknowledge input from the VMEbus
BBSY*	Bus Busy input from the VMEbus
BR3*	Bus Request 3 input for the VMEbus

68000 CPU signals

LD0 - LD15	Data lines from the 68000 CPU chip
LA1 - LA23	Address lines from the 68000 CPU chip
LAS*	Address Strobe signal from the 68000 CPU
LR/W	Read/Write signal from the 68000 CPU
LUDS*	Upper Data Strobe signal from the 68000 CPU
LLDS*	Lower Datat Strobe signal from the 68000 CPU
FC0 - FC2	Function code signals from 68000. Used to extend address space
IPL0 - IPL2	Interrupt Priority Level signal to 68000. Generate 7 interrupt levels
VMA*	Valid Memeory Address signal from 68000 to synchonous penpherals
LE	E strobe from 68000 to synchronous penpherals
DTCPU*	Data Transfer Acknowledge input to the 68000
CLOCK8	Divided CLOCK16 used by CPU, DRAM controller and DTACK PAL
LBERR*	Bus error input to the 68000 CPU
RESET*	Reset signal to all onboard circuits that require a reset
HALT*	Halt signal derived from reset and input to the 68000 CPU

Miscellaneous signals

CLOCK16	16 Mhz clock source for VMEbus SYSCLOCK the CPU clock
CLOCK2	Dived CLOCK16 used to generate BERR signal
RESIN*	Manual reset input to the TL7705A chip
CT	Time constant input to the TL7705A chip
REF	Input to the TL7705A chip
RESET	Reset signal source from the TL7705A chip
Z1-Z3	NOR gate outputs used to generate ZERO*
BERRCPU	Bus Error signal from 74164 shift register
AV1 - 7*	Auto Vector Interrupt lines used by onboard interrupt requestors
EOEI	Enable input for the 74348 offboard interrupt encoder
FPRST*	Reset signal to the Interface Processor board

Address Decoder PAL inputs

AV*	Low signal means the interrupt was from an onboard requester
FC*	Decode of FC0-2 indicating an interrupt acknowledge cycle
OFFBD*	Indicates an offboard address is present on the address lines
ZERO*	Used together with OFFBD* to detect the reset vector fetch

Address Decoder PAL outputs

CSDRAM*	Chip select for the 4502 DRAM controller chip (0x00008 to 0x7FFFF)
CSROM0*	Chip select for a 256kB bank of EPROM (0x80000 to 0xBFFFF)
CSROM1*	Chip select for a 192kB bank of EPROM (0xC0000 to 0xEFFFF)
CSRAM0*	Chip select for a 64kB bank of static RAM (0x100000 to 0x10FFFF)
CSRAM1*	Chip select for a 64kB bank of static RAM (0x110000 to 0x11FFFF)
PRPHA*	Common select for asynchronous peripherals (0xF0000 to 0xF7FFF)
PRPHS*	Common select for synchronous peripherals (0xF8000 to 0xFFFFF)
IJACK*	Interrupt acknowledge signal for off board interrupt service requests
VPA*	Valid Peripheral Address input to 68000

Asynchronous Address Decoder outputs

CSSIO1*	Chip select for MC68681 DUART used to communicate to front panel
CSSIO2*	Chip select for MC68681 DUART used for pROBE
CSGPIO*	Enables GPIO port buffers
CSADC*	Select for A/D convertor. Generates RDADC* and STRTADC*
CSDAC*	Latches data into the DAC
CSANL*	Latches data into a 74574 used to control the LED's and trigger
CSDFI*	Reset signal for the DFI circuit

Serial I/O signals

FPCLK	X1 clock from the Interface Processor board
FPCLK*	Inverted X1 clock from the Interface Processor board
FPRX	RX signal from the Interface Processor board
FPTX	TX signal to the Interface Processor board
SIO1CLK	Buffered 3.6864 MHz clock
SIO1CLK*	Buffered and inverted 3.6864 MHz clock
XTALSIO	Clock crystal input to MC68681 DUART
CLK3.68	3.6864 MHz clock source for MC68681 DUART
TxDB1	SIO port 1 channel B transmit signal
RxDB1	SIO port 1 channel B receive signal
CTSB1	SIO port 1 channel B Clear To Send signal
RTSB1	SIO port 1 channel B Ready To Send signal
TxDA2	SIO port 2 channel A transmit signal
RxDA2	SIO port 2 channel A receive signal
CTSA2	SIO port 2 channel A Clear To Send signal
RTSA2	SIO port 2 channel A Ready To Send signal
TxDB2	SIO port 2 channel B transmit signal
RxDB2	SIO port 2 channel B receive signal
CTSB2	SIO port 2 channel B Clear To Send signal
RTSB2	SIO port 2 channel B Ready To Send signal
TxDB1*	Inverted SIO port 1 channel B transmit signal
RxDB1*	Inverted SIO port 1 channel B receive signal
CTSB1*	Inverted SIO port 1 channel B Clear To Send signal
RTSB1*	Inverted SIO port 1 channel B Ready To Send signal
TxDA2*	Inverted SIO port 2 channel A transmit signal
RxDA2*	Inverted SIO port 2 channel A receive signal
CTSA2*	Inverted SIO port 2 channel A Clear To Send signal
RTSA2*	Inverted SIO port 2 channel A Ready To Send signal
TxDB2*	Inverted SIO port 2 channel B transmit signal
RxDB2*	Inverted SIO port 2 channel B receive signal
CTSB2*	Inverted SIO port 2 channel B Clear To Send signal
RTSB2*	Inverted SIO port 2 channel B Ready To Send signal
DTSIO*	Wire OR of dtack signals from the MC68681 chips

Synchronous Address Decoder outputs

CSRTC*	Select for RTC. Generates the ASRTC and DSRTC signals
CSRFCAL*	Select for the 68HC34 dual port RAM on the RefCal board

Miscellaneous Signal PAL outputs

RDADC*	Output buffer enable signal to the A/D convertor
STRTADC*	Signal used to gnerate the signal to start the A/D conversion
ASRTC	Address Strobe signal used to latch address into the RTC
DSRTC	Data Strobe signal used to read & write data to the RTC
LR/W*	Inveted R/W signal used to set direction of the RTC data buffer

VME Bus Arbitration PAL outputs

BGBD*	Bus Grant Board signal used to enable VMEbus drivers
ASBUS*	Address Strobe signal delayed for the VMEbus
ASBERR	Address Strobe Bus Error signal used to initiate bus error timeout
DTBUS*	Buffer DTACK* from the VMEbus

DRAM signals

MA0 - 8	Multiplexed Address signals from 4502 DRAM controller
RAS0*	Row Address Strobe 0 signal from DRAM controller
RAS0D*	RAS* passed through a series damping resistor
CAS0*	Column Address Strobe 0 signal from DRAM controller
CAS0U*	CAS0* ored with LUDS*. Used to select high byte
CAS0L*	CAS0* ored with LLDS*. Used to select low byte
CAS0UD*	CAS0UD* passed through a series damping resistor
CAS0LD*	CAS0LD* passed through a series damping resistor

Static RAM signals

WEU*	Write Enable Upper. LR/W ored with LUDS*
WEL*	Write Enable Lower. LR/W ored with LLDS*

Real Time Clock signals

VCCRTC	Power pin input for MC146818 RTC chip
OSC1RTC	Crystal oscillator input pin for RTC chip
OSC2RTC	Crystal oscillator input pin for RTC chip
XTALRTC	Node which attaches to top of 32.768 kHz crystal
PSRTC	Power Sense input to the RTC chip

Dynamic Fault Indicator Signals

DFIHIT	DFI timeout counter output
DFIHIT*	Open collector input to the CD4060 DFI timeout counter
DFI	Signal at the center of the DFI BNC
DFIOSC1	Oscillator 1 input to CD4060 DFI timeout counter
DFIOSC2	Oscillator 2 input to CD4060 DFI timeout counter

System trigger signals

SYNC_IN	System Sync signal input
SYNC_OUT	System Sync signal output

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK/DWB 5/24/88	WAVETEK SAN DIEGO, CALIFORNIA	
MATERIAL	PROJ ENGR Ed Ramo 6/88	TITLE	SCHEMATIC, 68000 VME BOARD
FINISH WAVETEK PROCESS	RELEASE APPROVAL Al Gillette	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030	
	DO NOT SCALE DWG	MODEL NO. 869	DWG NO. 1104-00-3409 REV A
	SCALE	CODE IDENT 23338	SHEET 7 OF 7

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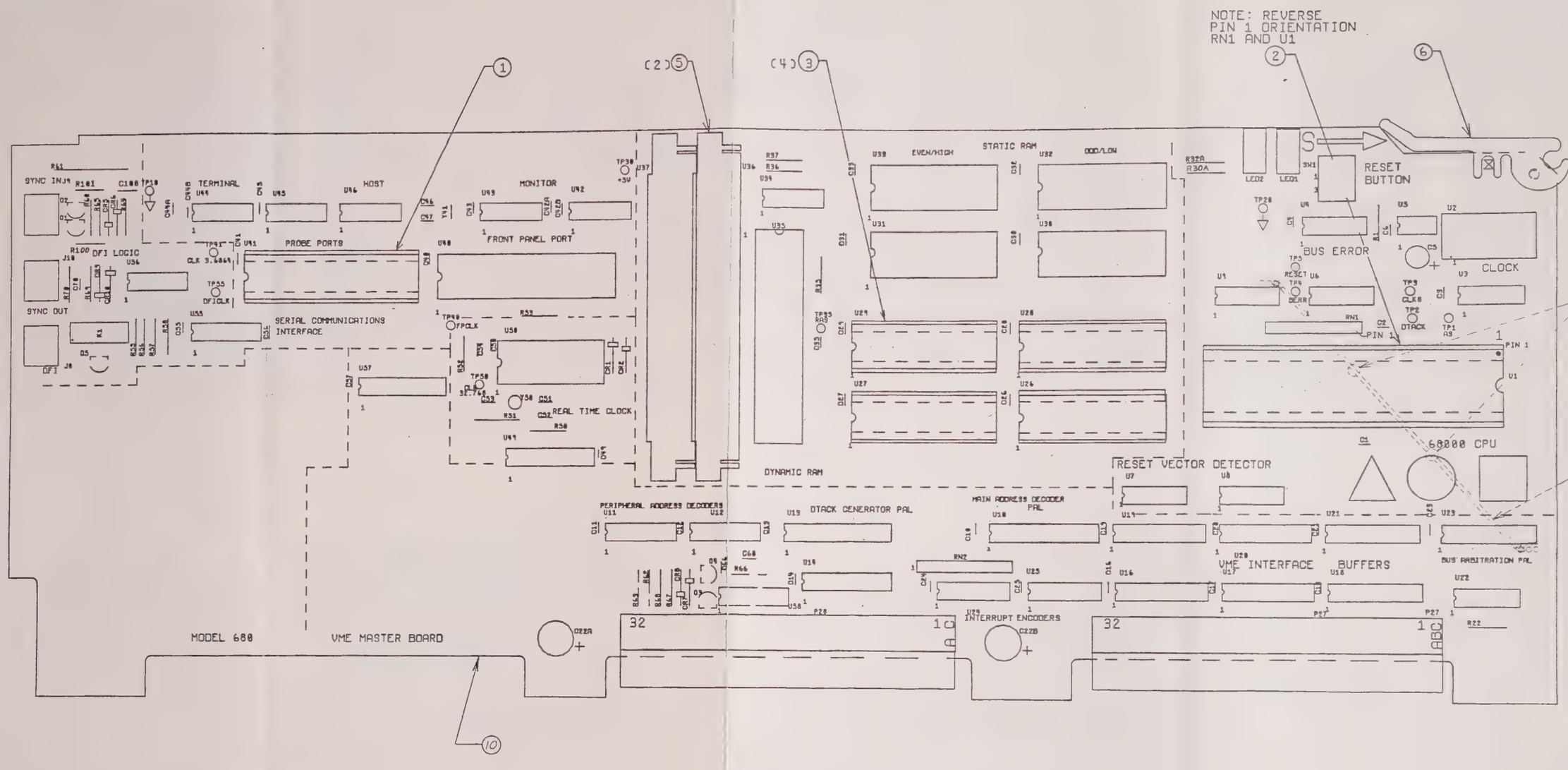
REV	ECN	BY	DATE	APP
A	REDRAWN USING DWG 1100-00-3127 ERO 90-434	S.C	6-23-90	



4. APPLY NON-CONDUCTIVE SILICONE (DOW CORNING RTV # 3140, OR EQUIV.) TO SECURE JUMPER WIRE TO PCA, AS REQUIRED.
3. ON SOLDER SIDE OF PCA INSTALL INSULATED 22 GAUGE JUMPER WIRE BETWEEN U23 PIN 8 AND U9 PIN 8.
2. REFERENCE DESIGNATORS DO NOT APPEAR ON PARTS.
1. SEE 1104-00-3409 FOR SCHEMATIC.

NOTE UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN RO FIFER/DMB	DATE 5/24/88	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL /	PROJ ENGR [illegible]	7-11-90	TITLE ASSEMBLY VME BOARD
	RELEASE APPROV [illegible]		
FINISH WAVETEK PROCESS /	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG		
	SCALE 1.75:1	MODEL NO 869	DWG NO 1101-00-3409 REV A
		CODE IDENT 23338	SHEET 1 OF 1

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REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	A/D VME BD-869	1101-00-3409	WVTK	1101-00-3409	1
NONE	SCHEMATIC VME BD-869	1104-00-3409	WVTK	1104-00-3409	1
C47	CAP,CER D18A,5PF,1KV,10%	CCD-050	ARCO	1500-00-5011	1
C68	CAP,CER,.001UF,1KV	D102K29Z5FNAAEM	PHLIP	1500-01-0211	1
C1 C10 C100 C11 C12 C13 C14 C16 C17 C18 C19 C2 C20 C21 C23 C24 C25 C26 C27 C28 C29 C3 C30 C31 C32 C33 C35 C4 C40 C41 C42A C42B C43 C44A C44B C45 C49 C50 C55 C57 C6 C66 C70	CAP CER MON .1MF 50V Z5U +80/-20% RAD LD SP .2 SP .2	SR215E104ZAA	AVX	1500-01-0420	43
C46 C53	CAP,CER,15PF,1KV	D150K20S2LNAAAL	PHLIP	1500-01-5011	2
C51 C52	CAP,CER,33PF,1KV	D330K29S2LNAAAL	PHLIP	1500-03-3011	2
C54	CAP,CER,.005MF,50V	CK-502	CRL	1500-05-0210	1
C5	CAP,ELECT,10MF/25V RADIAL LEAD, SP .10	NRE 10/63	NIC	1500-31-0002	1
C22A C22B	CAP,ELECT,100MF,35V RADIAL LEAD,SP .20	NRE101M35V10X12.5(OBS)	NIC	1500-31-0102	2
C56	CAP,MET,POLY,.01MF 100V 10% .2LS	103PMB100K(OBS)	IC	1500-41-0324	1
10	DRILL DRWG, 68000 VME	1700-00-2810	WVTK	1700-00-2810	1

WAVETEK PARTS LIST | TITLE PCA, VME BD | ASSEMBLY NO. 1100-00-3409 | REV C | PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	BD REF: SPEC 0008-00-0435 REV E				
J10 J8 J9	CONN, BNC(PC)	227161-1	AMP	2100-01-0019	3
P28	CONN,DINMRT ANGLE, PC MOUNT, 64 PIN A&C LOAD ROWS, 0.1 SPACING	D3M064RA27DS	HOLM	2100-02-0220	1
P27	CONN, DIN, MALE, 96 PIN, A/B/C,RTA	P196B30P00F00Z1	BURND	2100-02-0236	1
1	SKT,IC,40PIN	DILB40P-108T	BURND	2100-03-0030	1
2	SKT,IC,64 PIN	ICN-649B-S5-0	ROBNU	2100-03-007B	1
3	SOCKET,DUAL WIPE, 32 PIN	ICN-326B-S4-T	ROBNU	2100-03-0086	4
5	SOCKET,SINGLE STRIP,LOW PROFILE, 25 DEG	15-46-0051	MOLEX	2100-03-0089	2
TP1 TP10 TP2 TP20 TP3 TP30 TP35 TP4 TP40 TP41 TP5 TP50 TP55	TEST POINT, PC-TYPE	2100-04-0055	WVTK	2100-05-0024	13
Y50	CRYSTAL 32.768KHZ	KF38G	KYCRA	2300-99-0020	1
Y41	CRYSTAL, 3.6864MHZ	FOX036BS	FOX	2300-99-0029	1
U2	OCSILLATOR,CRYSTAL,TT	F1100-16.00 MHZ	FOX	2300-99-0031	1

WAVETEK PARTS LIST | TITLE PCA, VME BD | ASSEMBLY NO. 1100-00-3409 | REV C | PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	L,16MHZ, .01%				
6	PC BD EJECTOR	87-2-C	BRIT	2800-07-0032	1
K1	RELAY FORM C,SPDT,3W,ESD CNTL	RA30441051-02	ETROL	4500-00-0018	1
R51	RES,C,1/2W,5%,5.6M	RC-1/2-565J	STKPL	4700-25-5604	1
R64 R65 R70	RES,MF,1/8W,1%,100	RN55D-1000F	TRW	4701-03-1000	3
R1	RES,MF,1/8W,1%,1K	RN55D-1001F	TRW	4701-03-1001	1
R53 R57	RES,MF,1/8W,1%,10K	RN55D-1002F	TRW	4701-03-1002	2
R56	RES,MF,1/8W,1%,100K	RN55D-1003F	TRW	4701-03-1003	1
R30A R32A	RES,MF,1/8W,1%,10	5043ED10R100F	MEPCO	4701-03-1009	2
R50	RES,MF,1/8W,1%,150K	RN55D-1503F	TRW	4701-03-1503	1
R52	RES,MF,1/8W,1%,2K	RN55D-2001F	TRW	4701-03-2001	1
R100 R101 R60	RES,MF,1/8W,1%,21.5	RN55D-21R5F	TRW	4701-03-2159	3
R62 R63	RES,MF,1/8W,1%,301	RN55D-3010F	TRW	4701-03-3010	2
R68	RES,MF,1/8W,1%,332	RN55D-3320F	TRW	4701-03-3320	1
R35 R36 R37	RES,MF,1/8W,1%,33.2	RN55D-33R2F	TRW	4701-03-3329	3
R69	RES,MF,1/8W,1%,40.2	RN55D-40R2F	TRW	4701-03-4029	1

WAVETEK PARTS LIST | TITLE PCA, VME BD | ASSEMBLY NO. 1100-00-3409 | REV C | PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R67	RES,MF,1.8W,1%,46.4	RN55D-46R4F	TRW	4701-03-4649	1
R22 R55	RES,MF,1/8W,1%,4.75K	RN55D-4751F	TRW	4701-03-4751	2
R58	RES,MF,1/8W,1%,4.99K	RN55D-4991F	TRW	4701-03-4991	1
R66	RES,MF,1/8W,1%,82.5	RN55D-82R5F	TRW	4701-03-8259	1
R61	RES,MF,1/2W,1%,49.9	RN65D-49R9F	TRW	4701-23-4999	1
RN1 RN2	RES NETWORK 3.3K 2% 10PIN SIP BUSS	4310R-101-332	BOURN	4770-00-0023	2
CR1	DIODE, RECT, SCH BARRIER	MBR120P	MOT	4806-02-0120	1
CR10 CR9	DIODE, ULTRA FAST	1N4244	T/CSF	4807-02-0777	2
CR2 CR5 CR6 CR7 CR8	DIODE 5082-2811 SCHOTTKY,15V,20MA	5082-2811	HP	4809-02-2811	5
G3 G4	TRANS, NPN, TO-92	PN3563	NSC	4901-03-3630	2
G5	TRANS 2N3906 PNP GENERAL PURPOSE TO-92	2N3906(OBS)	FAIR	4901-03-9060	1
G1 G2	TRANS 2N5771 PNP SWITCH TO-92	2N5771	NSC	4901-05-7710	2
SW1	SWITCH, PUSHBUTTON, PCB	BB600	CUTHM	5199-00-0011	1
U5	RESET GEN	TL7705ACP	TI	7000-77-0501	1

WAVETEK PARTS LIST | TITLE PCA, VME BD | ASSEMBLY NO. 1100-00-3409 | REV C | PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U30 U31 U32 U33	BAT BACKED,32K X 8	DS1235Y	DALAS	8000-12-3500	4
U42 U44	RS-232C QUAD LINE DRIVER	MC1488P	MOT	8000-14-8800	2
U43 U45	RS-232C QUAD LINE RECEIVER	MC1489L	MOT	8000-14-8900	2
U55	COUNTER, 14 BIT, OSC, CMOS	CD4060BE	RCA	8000-40-6000	1
U35	CONTROLLER, DYNAMIC RAM	THCT4502JD	TI	8000-45-0200	1
U56	GATE, NAND, QUAD 2-INPUT POS W/OC OUTPUTS	SN7401N	TI	8000-74-0100	1
U46	HEX INVERTER	SN74ALS04BN	TI	8000-74-0402	1
U6	HEX INVERTER W/OC	SN74ALS05AN	TI	8000-74-0501	1
U9	GATE, NAND, DUAL 4 IN	SN74ALS20AN	TI	8000-74-2001	1
U34	GATE, OR, QUAD 2 IN ROS	N74F32N	SIG	8000-74-3200	1
U38	TRANSLATOR,QUAD TTL-TO-MECL	MC10H124P	MOT	8001-01-2401	1
U36 U37	DRAM,256KX8,100NS,SIM M	TM4256GUS-10L(OBS)	TI	8002-56-0801	2

WAVETEK PARTS LIST | TITLE PCA, VME BD | ASSEMBLY NO. 1100-00-3409 | REV C | PAGE 5

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U1	MICROPROC 16 BIT 10 MHZ	MD68000-10	HTACH	8006-80-0000	1
U40	UART DUAL	MC68681P	MOT	8006-86-8100	1
U11 U12	DECODER/DEMUX, 3 TO 8 LINE	SN74ALS138N	TI	8007-41-3800	2
U4	REG, SERIAL SHFT, 8 BIT PAR OUT	SN74LS164N	TI	8007-41-6401	1
U7 U8	DIGITAL TTL	74F260PC	FAIR	8007-42-6000	2
U24 U25	ENCODER, 8 TO 3 LINE PRIOR, W/3 STATE	SN74LS348N	TI	8007-43-4800	2
U3	COUNTER,DUAL DECADE,4 STG BIN	8007-43-9300	WVTK	8007-43-9300	1
U57	FLIP-FLOP, OCTAL D	SN74ALS574N	TI	8007-45-7450	1
U16 U17 U18 U19 U20 U21 U49	TRANSCEIVER, OCTAL BUS W/3 STATE	SN74ALS645A-1N	TI	8007-46-4500	7
U50	REAL TIME CLOCK	MC146818P	MOT	8014-68-1801	1
U22	BUFF, HEX NONINVERT W/OC	SN74ALS1035N	TI	8074-10-3500	1
U13	PAL PROG, USES 1 EA 6000-20-4000 FOR MODEL 680 VER 1.0	B600-00-0447	WVTK	8600-00-0447	1

WAVETEK PARTS LIST | TITLE PCA, VME BD | ASSEMBLY NO. 1100-00-3409 | REV C | PAGE 6

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE: PARTS LIST 68000 VME BOARD
	PROJ. ENGR.		
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D · FSCM NO. 23338 · DWG. NO. 1100-00-3409 · REV C · SCALE · MODEL 869 · SHEET 1 OF 2

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REV	ECO	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U14	PAL, PROG, USES 1 EA 8000-16-8000 FOR MODEL 680 VER 1.0	8600-00-0448	WVTK	8600-00-0448	1
U10	PAL, PROG, USES 1 EA 8002-01-0000 FOR MODEL 680 VER 2.0	8600-00-0449	WVTK	8600-00-0449	1
U26	EPROM PROGRAM SET, USES 1 EA 8002-75-1200	8600-00-0603	WVTK	8600-00-0603	1
U27	EPROM PROGRAM SET, USES 1EA 8002-75-1200	8600-00-0604	WVTK	8600-00-0604	1
U23	GAL, PROG, USES 1EA 8000-16-8002 FOR MOD 680	8600-00-0606	WVTK	8600-00-0606	1
U29	PROG, EPROM, USES 8002-75-1200 FOR MOD680, REF U29, V1.2.0	8600-00-0734	WVTK	8600-00-0734	1
U28	PROG, EPROM, USES 8002-75-1200 FOR MOD 680, REF U28, V1.2.0	8600-00-0735	WVTK	8600-00-0735	1

WAVETEK PARTS LIST	TITLE PCA, VME BD	ASSEMBLY NO. 1100-00-3409	REV C
		PAGE 7	

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE
MATERIAL	CHECKED	
	PROJ. ENGR.	
	RELEASE APPROV.	
FINISH WAVETEK PROCESS	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± .XXX ± ±	
DO NOT SCALE DRAWING		

WAVETEK SAN DIEGO, CALIFORNIA

TITLE
PARTS LIST
68000 VME BOARD

SIZE	FSCM NO.	DWG. NO.	REV
D	23338	1100-00-3409	C

SCALE | MODEL 869 | SHEET 2 OF 2

MP MASTER
MA35705